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ION IMPLANTED GaAs I.C. PROCESS TECHNOLOGY

Quarterly Technical Report No. 7

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report covers the second quarter, Phase II of a program on ion implanted planar GaAs integrated circuit technology. The overall objective of this program is the development of a manufacturable process for high-speed low-power GaAs logic circuits. The goal for Phase I was to establish the technology, and demonstrate its viability by fabricating circuits reaching MSI complexity. The goal for Phase II is to achieve the capability of fabricating GaAs ICs of LSI complexity. The program involves the Rockwell International Electronic Research Center and three subcontractors; Crystal

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Specialties Inc., the California Institute of Technology and Cornell University.

) The most important result in this quarter was the successful demonstration of an 8:1 data multiplexer and a 1:8 data demultiplexer operating at clock rates as high as 1.1 GHz. In addition, operation of ÷8 circuits has been observed at frequencies as high as 1.9 GHz. Thus, the design objective for the operating speed of these demonstration circuits has been achieved.

Having the design goals for mask set AR2 accomplished, considerable attention was given to the design and layout of mask set AR3. This mask set contains two new circuits, a 3-bit x 3-bit parallel multiplier and a 1 x 8 stage shift register. Results obtained from evaluation of those circuits will provide the basis for design of the larger parallel multiplier and shift register circuits that will be used to demonstrate the capability of fabricating GaAs ICs having 500-1000 gates. In addition, the mask set contains redesigned versions of the 8:1 data multiplexer and the 1:8 data demultiplexer, resulting in an increase in the gate count of the demultiplexer to 103. The process monitor test patterns have also been redesigned. Digitization of this mask set has been completed, and fabrication of the first wafers is expected shortly.

Work on all other aspects of the program has continued. Recent data on outdiffusion of chromium from semi-insulating GaAs during annealing, obtained under an IR&D program, may be helpful in understanding the results of qualification tests in that material. Electron concentration profiles have been measured by C-V techniques in qualification samples which exhibited an n-type surface layer following the isolation tests. These profiles are consistent with the expected results if chromium outdiffusion occurred to such an extent that a constant donor background was no longer compensated.

Contact resistance data on a number of IC wafers have recently been evaluated. The results indicate a steady trend toward lower contact resistance as the program progresses. Specific contact resistance values of the order of x 2 10^{-6} Ω-cm^2 are being achieved at the present.

The saturation current for neighboring FETs and active loads in the T2 test patterns have been correlated using the automatic measurement system in order to determine whether the short range fluctuations of device parameters are smaller than the long range variations. The results show that the short range variations on most of the wafers are of the same order as the long range variations observed on the wafers showing the best uniformity. Long chains of 98 NOR gates employing 5 μm wide FETs were also tested. A yield of 50% fully working chains was observed on a test wafer.

Device modeling work at Cornell has been extended to take into account the shape of the ion implantation profile (an abrupt profile has been previously used) in the FET model. This refinement has led to better matching with the device characteristics at high saturation currents. A hybridization of this model with Shockley's model, adapted for a nonuniform profile, is expected to improve the fit in the low current region, near pinchoff.

FOREWORD

The research covered in this report is carried out in a team effort having the Rockwell International Electronics Research Center as the prime contractor with two universities and a crystal manufacturer as subcontractors. The effort is sponsored by the Materials Science Office of the Defense Advanced Research Projects Agency. The contract is monitored by the Air Force Office of Scientific Research. The Rockwell program manager is Fred A. Blum. The principal investigators for each organization are:

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California Institute of Technology	J. A. Mayer, M. A. Nicolet
Cornell University	L. F. Eastman
Crystal Specialties	W. P. Allred

Numerous other researchers are involved in the work reported on. The principal contributors are:

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Cornell University	M. Shur
Crystal Specialties	J. Burns, H. Olsen

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TECHNICAL SUMMARY

This report covers the second quarter, Phase II, of the program on ion implanted planar GaAs integrated circuit technology. The goal for Phase II of the program is to achieve the capability of fabricating GaAs ICs of LSI complexity. The fabrication approach, demonstrated in Phase I, is based on multiple localized implantations directly into the semi-insulating GaAs substrate to form active device areas insulated by the unimplanted regions of the substrate. The circuit concept, also demonstrated in Phase I, involves a combination of Schottky diodes and depletion mode Schottky barrier FETs (SDFL), employed to form logic gates capable of high speed operation with very low power.

This program requires a research effort on all the multiple facets of process development. The research activities range from substrate growth and ion implantation technology to fabrication and evaluation of test circuits. These activities are carried out by the Electronics Research Center with the support of three subcontractors, Cal Tech, Cornell University, and Crystal Specialties, Inc.

The most important result in this quarter was the demonstration of the operation of an 8:1 data multiplexer and an 1:8 data demultiplexer at clock rates as high as 1.1 GHz. In addition, operation of a ÷8 circuit has been observed at frequencies as high as 1.9 GHz.

The following is a summary of the accomplishments of the program in the past quarter.

Semi-Insulating Substrate Material (Section 2.0)

Crystal Specialties have continued supplying the qualified semi-insulating substrate material required by the program. The yield has been similar to that of previous quarters. Difficulties with inclusions in portions of the grown ingots reappeared. Attempts to overcome this problem by improving boat cleaning procedures and by varying the stoichiometry of the

melt are currently being pursued. Bulk chemical analysis of a number of grown ingots was performed using the SIMS technique. Large variation of chromium concentrations from ingot to ingot were observed despite the fact that the amounts of chromium added to the melt were comparable for all the ingots. Since the oxygen content of the growth ampoule could affect the chromium incorporation, plans are being made for growth runs with tighter control of the oxygen content in the growth ampoule.

The expanded qualification procedures described in the last Quarterly Report (which include the Kr^+ bombardment test, the isolation test, and the examination of carrier density profiles for typical FET channel implants) were continued during this period with satisfactory results. Based on the shape of the carrier density profiles the qualified material is now being classified into type A and type B, type A exhibiting the narrowest profile, and being favored in the IC process.

The photo-induced transient spectroscopy (PITS) technique has been used to survey a variety of samples from ingots grown by Crystal Specialties. The result is a tabulation of deep levels observed in the material. SIMS investigations of heat treated substrates (conducted under an IR&D program) indicate a significant redistribution of chromium when the substrate is capped and annealed, showing accumulation of chromium near the cap-GaAs interface, and depletion of chromium in the bulk over a distance of several microns from the interface. A model attributing the formation of an n-type layer in unqualified substrates to lack of compensation due to chromium depletion has been suggested.

Planar Process Development (Section 3.0)

A study of silicon implantation for achieving high doping density in GaAs with a process compatible with the low dose implantations has continued. By comparing carrier concentration profiles with the results of SIMS silicon profiles it was concluded that the observed limit of $n_e = 2 \times 10^{18}$ cm^{-3} is a consequence of incomplete activation of the implanted silicon. The hy-

pothesis that the incomplete activation is due to the formation of neutral Si_{Ga}-Si_{As} nearest neighbor pairs has been advanced.

Some wafers were processed from an ingot appraised as marginal during the qualification test. The data from isolation test patterns showed high leakage currents, and the I-V characteristics of test FETs displayed unusually high pinchoff voltage. This test has provided information on ingots which qualified with marginal success, and has demonstrated that the overall qualification procedures used in this program are adequate to predict the quality and usefulness of a particular GaAs ingot.

Ohmic contact resistance data on a number of IC wafers have recently been evaluated. The results indicate a steady trend toward lower contact resistance as the program progresses. Specific contact resistance values of the order of 2×10^{-6} Ω-cm^2 are being achieved at present.

Circuit Performance (Section 4.0)

Measurement of capacitance-voltage profiles can now be carried out automatically on the probe station used for low frequency device characterization. This will facilitate routine determination of the implantation doping profiles on fabricated wafers. The saturation current for neighboring FETs and active loads in the T2 test patterns have been correlated using the automatic measurement system in order to determine whether the short range fluctuations of device parameters are smaller than the long range variations. The results show that the short range variations on most wafers are of the same order as the long range variations observed on the wafers showing the best uniformity. Long chains of 84 and 98 NOR gates employing 5 μm wide FETs were also tested. A yield of 50% fully working chains was observed on a test wafer.

As mentioned earlier in this summary, the most important results in this quarter were obtained by testing the multiplexer and demultiplexer, and also some ÷8 circuits on new wafers fabricated with the AR2 mask set. While in the previous quarter only low speed operation of the multiplexer and de-

multiplexer was demonstrated, with the new measurements operation of the 8:1 data multiplexer and 1:8 data demultiplexer at clock rates as high as 1.1 GHz has been attained, while operation of ÷8 circuits have been observed at frequencies as high as 1.9 GHz. The equivalent propagation delay is as low as 110 ps/gates. Since the ÷8 circuit contains gates with fanouts of 2-4 and is a sequential logic circuit, this high speed performance clearly shows that the SDFL circuit approach is not limited to low speeds or low fanout and is competitive in speed to buffered FET logic designs while requiring significantly less power.

Circuit Design (Section 5.0)

Design and digitization of the AR3 mask set which contains demonstration circuits for the next stage of development in this program has been completed, and fabrication of the first wafers is expected to begin shortly. Mask set AR3 contains two new circuits, a 3-bit by 3-bit parallel multiplier and a 1 × 8 stage shift register. Results obtained from evaluation of these circuits will provide the basis for design of the larger parallel multiplier and shift register circuits that will be used to demonstrate the capability of fabrication GaAs ICs having 500-1000 gates. In addition, the mask set contains redesigned versions of the 8:1 data multiplexer and the 1:8 data demultiplexer, resulting in an increase in the gate count of the demultiplexer to 103.

The process monitor test patterns have also been redesigned in AR3 eliminating some test patterns that are no longer necessary, refining the design of others, adding some new test patterns, and incorporating test patterns that were previously in the PD chip no longer in use.

Device modeling work at Cornell has been extended to take into account the shape of the ion implantation profile in the FET model leading to better fit to the device characteristics at high saturation current. A hybridization of this model with Schockley's model adapted for a nonuniform profile is expected to improve the fit in the low current region, near pinchoff.

1.0 INTRODUCTION

This report covers the second quarter, Phase II of a program on ion implanted planar GaAs integrated circuit technology. The objective of this program is the development of an integrated circuit process technology for GaAs taking advantage of its superior electrical properties in order to achieve high speed low power digital integrated circuits. The goal for Phase I was to establish the technology, and demonstrate its viability by fabricating circuits reaching MSI complexity.[1] The goal for Phase II is to achieve the capability of fabricating GaAs ICs of LSI complexity. The bulk of the work on this program is carried out at the Rockwell International Electronics Research Center. Significant assistance is provided by three subcontractors; Crystal Specialties Inc., California Institute of Technology, and Cornell University.

In the previous quarter, proper operation of the multiplexer and demultiplexer circuits from mask set AR2 was reported. The speed of operation was rather low for this high-speed technology. The most important results in this quarter were obtained by testing the multiplexer and demultiplexer and also some ÷8 circuits on new wafers fabricated with the AR2 mask set. Operation of the 8:1 data multiplexer and 1:8 data demultiplexer (both with >60 gates each) has been attained at clock rates as high as 1.1 GHz. In addition, operation of ÷8 circuits (25 gates) has been observed at frequencies as high as 1.9 GHz, corresponding to propagation delays as low as 110 ps/gate. Since the D flip-flop chain contains gates with fanouts of 2 to 4 and is a sequential logic circuit, this high speed performance clearly shows that the SDFL circuit approach is not limited to low speeds or low fanouts and is competitive in speed to buffered FET logic designs while requiring significantly less power.

Having accomplished the design goals for mask set AR2, considerable attention was given to the design and layout of mask set AR3. This mask set contains two new circuits, a 3-bit × 3-bit parallel multiplier and a 1 × 8

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Contact resistance data on a number of IC wafers have recently been evaluated. The results indicate a steady trend toward lower contact resistance as the program progresses. Specific contact resistance values of the order of 2×10^{-6} Ω-cm^2 are being achieved at the present.

Acquisition of capacitance-voltage data can now be carried out automatically on the low frequency probe station. This will facilitate routine determination of implantation doping profiles on fabricated wafers. The saturation current for neighboring FETs and active loads in the T2 test patterns have been correlated using the automatic measurement system in order to determine whether the short range fluctuations of device parameters are smaller than the long range variations. The results show that the short range variations on most of the wafers are of the same order as the long range variations observed on the wafers showing the best uniformity. Long chains of 84 and 98 NOR gates employing 5 μm wide FETs were also tested. A yield of 50% fully working chains was observed on a test wafer.

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2.0 MATERIALS

This section reviews the progress achieved in the area of supply and characterization of semi-insulating GaAs substrate material. Crystal growth activities at Crystal Specialties are first reported, followed by the qualification results obtained at the Electronics Research Center for the grown ingots. Finally, analytical work directed at further understanding of the behavior of semi-insulating GaAs is described.

2.1 Bulk Growth of Semi-insulating GaAs (Crystal Specialties and Electronics Research Center)

The single crystal yield (fraction of growth starts which produced high quality single crystals) continued at an acceptable level (74%), indicating a low incidence of the boat-wetting problem which affected crystal growth in the past. Similarly, the compensation yield (fraction of Cr doped single crystal ingots which were semi-insulating) remained high (90%). Difficulties with inclusions in a portion of the grown ingots reappeared, however. Attempts to overcome this problem by increasing care in cleaning the growth boat after sandblasting and by varying the stoichiometry of the melt are currently being pursued.

At the suggestion of S. Roosild (RADC), bulk chemical analysis of seed and tail end samples of a number of grown ingots was performed using the SIMS technique (at Charles Evans & Associates, San Mateo, Ca.). Although the exact calibration of the resulting concentrations is currently uncertain, several interesting results were obtained by comparing relative concentrations in various samples. For example, a substantial variation of Cr concentration was found among the samples examined. For a given ingot, the Cr concentration was typically 1.5 to 2.5 times higher at the tail end of the ingot than at the seed end. This variation is consistent with normal Cr incorporation in the growing crystal, since the Cr distribution coefficient is known to be low ($\sim 6 \times 10^{-4}$), and the tail samples were taken from a region approximately 1/2

to 2/3 of the total length of the ingot (due to ingot cropping) distant from the seed end. In several ingots the overall Cr content was abnormally high (twice the typical value), although the amount of Cr added to the melt was comparable for all the ingots. A possible mechanism for the increased Cr incorporation could be variation in the O_2 content of the growth ampoule, either through the formation of Cr-O complexes or through variations in the concentration of residual donors (typically silicon resulting from the dissociation of SiO_2 - a reaction which itself depends on the O_2 content of the system). Currently, plans are being made to regulate the amount of O_2 in the system by baking out the Ga source material in H_2 prior to growth, and subsequently backfilling the ampoule with a metered amount of O_2. This bakeout should also contribute toward a reduction in the impurity content of the source material.

On the basis of the initial SIMS results, no clear correlation between the Cr concentration in an ingot and its qualification for ion implantation could be established.

2.2 Substrate Evaluation (Electronics Research Center)

The expanded qualification procedures described last quarter (which include the Kr^+ bombardment test, the isolation test, and the examination of carrier density profiles for typical FET channel implants) were continued during this period.[2] Of five ingots grown by Crystal Specialties, two were found to be qualified for use in ion implantation, for a yield of 40%.

The recently instituted implantation profile test has proved to be a sensitive measure of ingot performance. On the basis of the results of this test, a classification for qualified ingots has been instituted. Accordingly, the ingots which display relatively deep carrier profiles after the standard Se implant are designated type B, while those with the narrowest profiles are designated type A. Currently, type A substrate material is favored in the IC process. During this quarter, one of the two qualified ingots examined was type A while the remaining one was type B. Over the last nine months, of the twelve qualified ingots examined, ten (88%) were type A, and two (12%) were type B.

2.3 Analysis of Semi-Insulating GaAs (Electronics Research Center)

Further characterization of the deep level concentrations in semi-insulating GaAs was carried out using the photo-induced transient spectroscopy (PITS) technique. As described in earlier reports,[1,2] this technique makes use of trap-induced photoconductivity transients to detect the presence of deep electron states in the material and to evaluate their emission cross sections. During this quarter, a survey of samples (from both front and tail ends) of ingots grown by Crystal Specialties was completed. A large fraction of the trap levels detected were found to be common to more than one ingot. An inventory of the trap levels found is shown in Table 2.3-1. In this table, traps are listed by the temperature at which their emission rate coincides with the 3 msec rate window used in the survey. Trap activation energies and cross sections are also shown; these were determined by using successive scans varying the rate window as in the DLTS method. Deep levels corresponding to Cr and O are expected to have PITS peaks at temperatures above the 400°C maximum temperature of the scans used in earlier work. Accordingly, the substrate holder was redesigned to permit extension of the data to 500°C. Preliminary results suggest observation of the Cr hole trap level at $E_{act} = 0.9$ eV.

In addition to the SIMS analysis of bulk material described in Section 2.1, SIMS investigations of heat treated substrates conducted under an IR&D program have a bearing on the understanding of substrate qualification, and will be summarized here. The SIMS profiles (measured by Charles Evans & Associates) indicated that significant redistribution of Cr occurs when substrates of semi-insulating GaAs are capped with reactively sputtered Si_3N_4 and annealed. Chromium appears to accumulate in the vicinity of the cap - GaAs interface. As a result, the Cr concentration is reduced from its bulk value over a distance of several microns from the interface. Except within 1000A of the interface, the measured Cr profiles were well described by a complementary error function fit corresponding to simple diffusion; the diffusion coefficient was found to be approximately 10^{-11} cm^2/sec at 850°C. The Cr profiles were found to be similar for qualified and unqualified samples; the profile

Table 2.3-1 Deep Levels in SemiInsulating GaAs

T_m (°K)	E_t (eV)	S_n (cm^2)	3921F	3921T	3897F	3897T	3992F	3992T	3948F	3805T	3608T	3552T
75	-	-						x				
90	0.15	4×10^{-14}	x			x		x			x	x
92	0.18	1×10^{-12}	x									
108	-	-						x				
117	0.14	1×10^{-16}	x						x			
126	0.26	2×10^{-12}	x	x		x		x	x		x	x
149	0.30	9×10^{-13} ($S_p = 7 \times 10^{-14}$)				x		x				x
170	0.34	6×10^{-13}	x	x	x		x		x	x		x
190	0.34	4×10^{-14}				x		x				
202	0.26	1×10^{-16}	x	x		x	x		x	x	x	x
210	0.40	5×10^{-14}				x		x				
249	0.51	1×10^{-12}	x	x		x	x					
274	0.60	2×10^{-12}	x	x	x	x	x	x	x	x		x
328	-	-						x				
370	0.82	2×10^{-12}				x		x				
425-445	0.90	$S_p = 3 \times 10^{-14}$	x	x	x	x	x	x	x	x	x	x

T_m is the temperature at which the PITS signal is maximized for a 3 msec rate window; E_t is the trap activation energy, and $S_n(S_p)$ is its capture cross section for electrons (holes).

shape was also found to be unchanged by implantation of Kr or Se ions at low doses (< 3×10^{12} cm^{-2}).

The depletion of Cr over a significant depth near the surface of the substrates might be expected to have an important effect on the electrical compensation of the samples. Since ingots typically contain a background concentration of residual donors which are normally compensated by the Cr centers, a Cr deficient region could become undercompensated and thus n-type. To confirm this, carrier density profiles were measured using the C-V technique in unqualified GaAs samples that had been capped and annealed. Such profiles showed the formation of an n-type surface layer. It was found that the tail region of the carrier distribution correlated very well with the results expected from Cr out-diffusion. The profiles also suggested that an additional mechanism (currently unknown) contributes to the n-type layer in some samples.

On the basis of these results, a model has been formulated to explain the variations in electrical behavior among different ingots of semi-insulating GaAs due to the Cr mechanism. It is postulated that qualified ingots have a low concentration of residual donors or high concentration of Cr, so that any n-type layer resulting from Cr migration is so thin that it is fully depleted due to pinning of the Fermi level at the surface and in the bulk. On the other hand, unqualified ingots have a particularly high concentration of the residual donors, resulting in a wide, heavily n-type layer after the anneal.

3.0 PLANAR PROCESS DEVELOPMENT

Several aspects of process development are covered in this section. Section 3.1 contains a discussion of recent work at Caltech on Si implantations including possible causes for the observed ceiling on achievable carrier concentrations. Section 3.2 contains a discussion of doping profiles for test chips processed in parallel with IC wafers and shows the results from processing IC wafers on unqualified substrate material. Finally, Section 3.3 presents results from ohmic contact specific resistance measurements showing remarkable progress from the beginning of the program.

3.1 Ion Implantation (Caltech and Electronics Research Center)

This section contains reults on semi-insulating GaAs wafers implanted at Caltech with 300 keV Si^+ ions at room temperature to doses in the range 10^{13} - 2×10^{15} cm^{-2}. Capping with reactively sputtered silicon nitride and furnace annealing for 30 min at 50°C intervals from 700° to 950°C in a hydrogen ambient were carried out at Rockwell International Electronics Research Center. Ohmic contacts and van der Pauw patterns were prepared by Rockwell. Depth profiles of the free electron concentration and of the electron mobility were then measured at Caltech by means of the anodic stripping method. The previously reported electron concentration (n_e) profiles and an upper achievable limit of $n_e = 2 \times 10^{18}$ cm^{-3} have been confirmed.[3] Detailed profiles of electrical activity are now available for the full range of implantation doses and anneal temperatures given above. In addition, atomic depth profiles for Si and Cr have been obtained by the SIMS technique and a hypothesis advanced to explain the experimental results.

A comparison of free electron concentration profiles with calculated LSS atomic profiles for Si is shown in Fig. 3.1-1, for a dose range between 5.7×10^{13} cm^{-2} and 1×10^{15} cm^{-2} and annealing at 850°C and 900°C. The maximum achievable free electron concentration is $n_e \approx 2 \times 10^{18}$ cm^{-3}, independent of implanted dose or anneal temperature. From these and the other measured

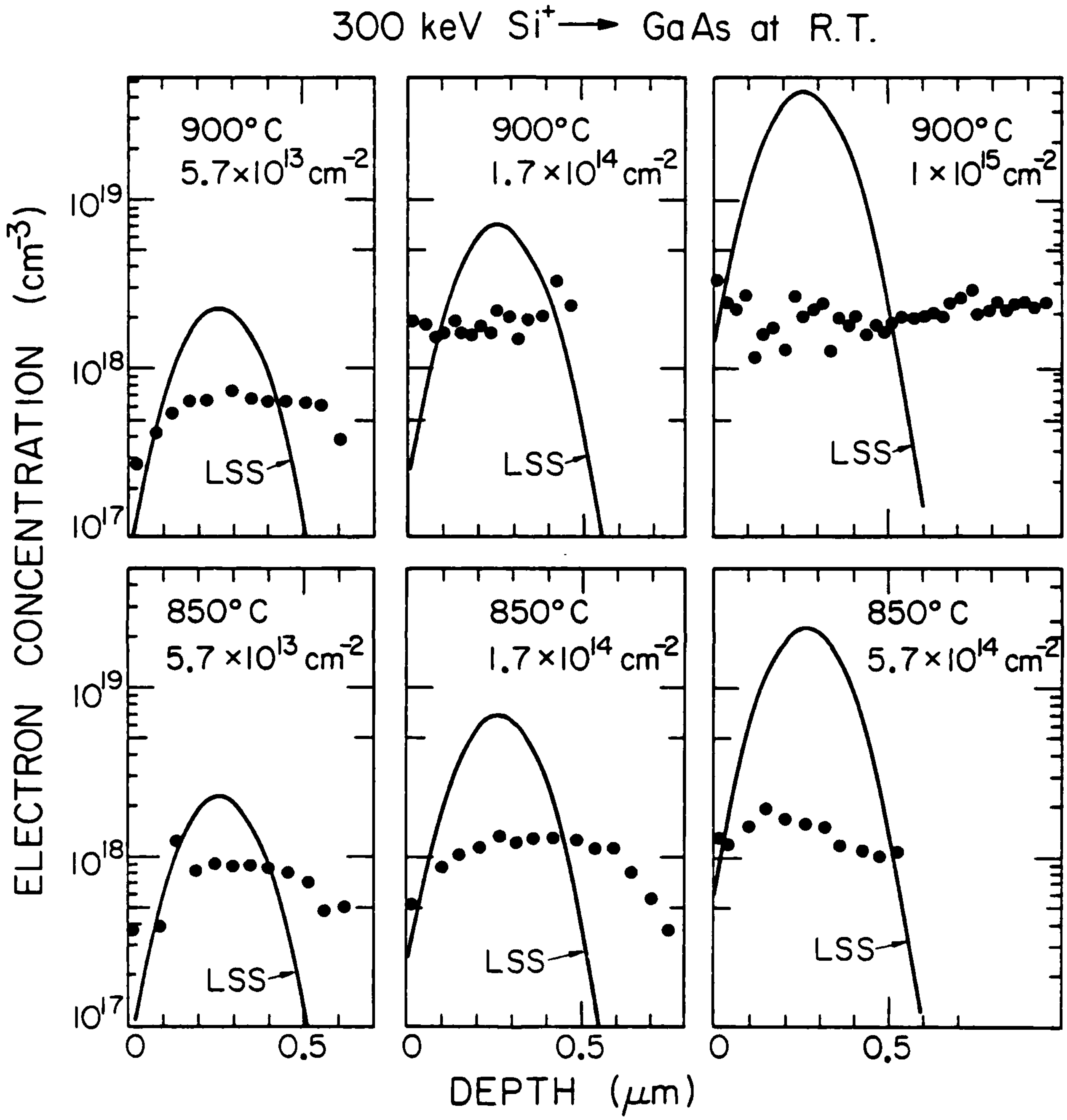

Fig. 3.1-1 Comparison of free electron concentration profiles with calculated LSS atomic profiles for Si implants.

profiles (not shown) the following conclusion can be drawn. The higher the implanted Si dose and the higher the anneal temperature (for $T_{anneal} > 850°C$) the flatter and the deeper are the n_e profiles, as compared to computed LSS atomic profiles. To determine whether or not this effect is due to Si diffusion, SIMS measurements have been carried out. As seen in Figs. 3.1-2 and 3.1-3, the Si atomic profiles thus obtained do not account for the observed electron profiles, since Si is still present in concentrations larger than n_e after annealing. Furthermore, the atomic Si profile is not flat as is the n_e profile. The limit of $n_e \approx 2 \times 10^{18}$ cm^{-3} is thus a consequence of incomplete activation of the implanted Si.

An additional interesting observation is that Cr, which is normally uniformly distributed in the grown GaAs crystal, tends to move to the surface during the anneal. The atomic Cr profiles roughly follow the Si profiles, but still do not account for the shape or the magnitude of the electron concentration profiles, unless a non-linear compensation behavior of Si by Cr is invoked. Therefore a different hypothesis is proposed to explain the results. The relatively low fraction of electrically active Si in high-dose implants may be due to the formation of neutral Si_{Ga}-Si_{As} near-neighbor pairs. Such pairs have been identified previously by infrared absorption spectroscopy[4] and they are expected to form most readily at high Si concentrations. The results of mobility measurements are consistent with this hypothesis. In Fig. 3.1-4, the observed electron mobility is plotted as a function of both the implanted dose (N_d) and the electrically active dose (N_s). The electron mobility is seen first to decrease with increasing Si implant dose, as would be expected when the implanted Si is elecrically active. However, for doses $> 10^{15}$ cm^{-2} and anneal temperatures $< 850°C$, the mobility increases again. This behavior suggests a reduction in the number of scattering centers; the mobility is generally dominated by ionized impurity scattering at these high doping levels.

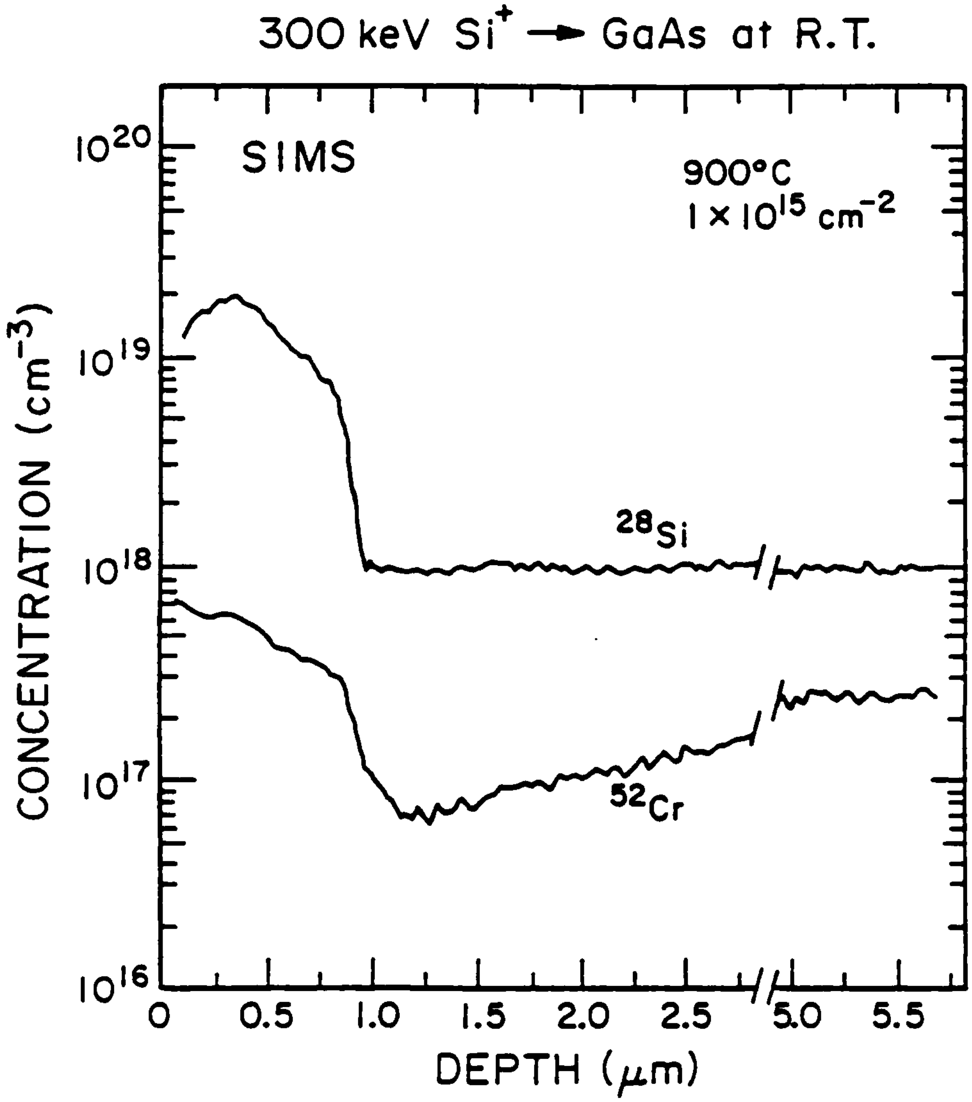

Fig. 3.1-2 SIMS profiles for Si implanted GaAs.

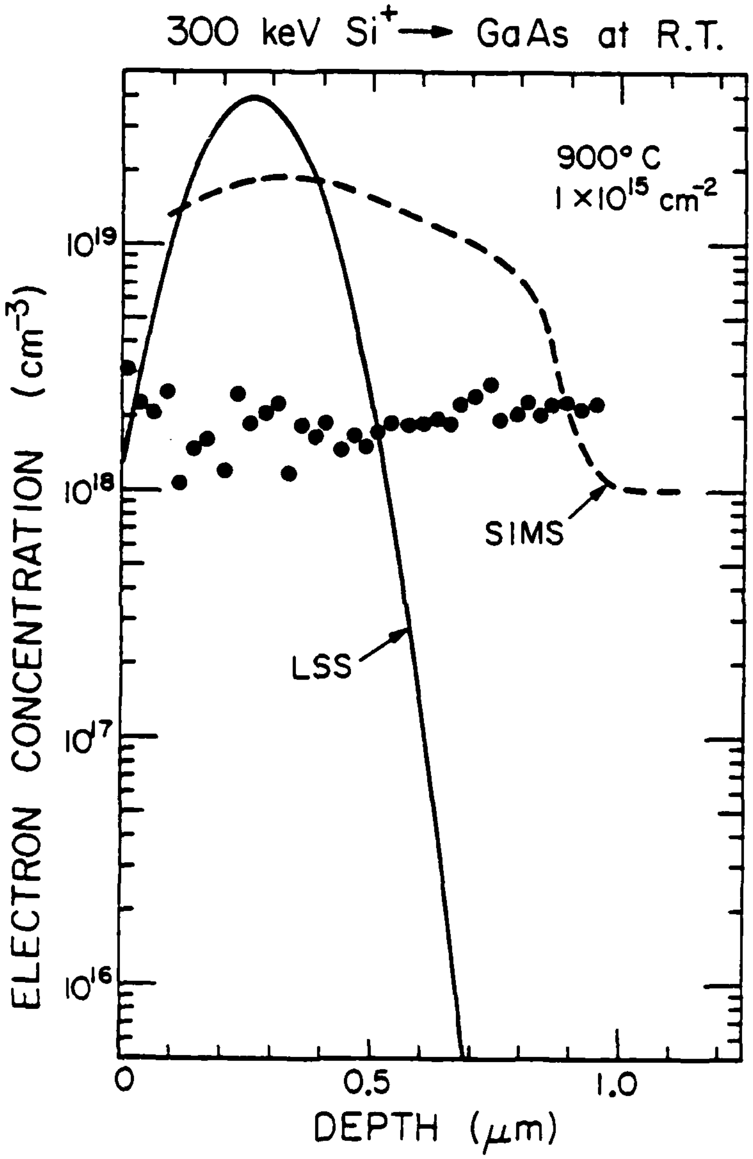

Fig. 3.1-3 Comparison of the free electron concentration profile with the Si ion concentration profile obtained by SIMS.

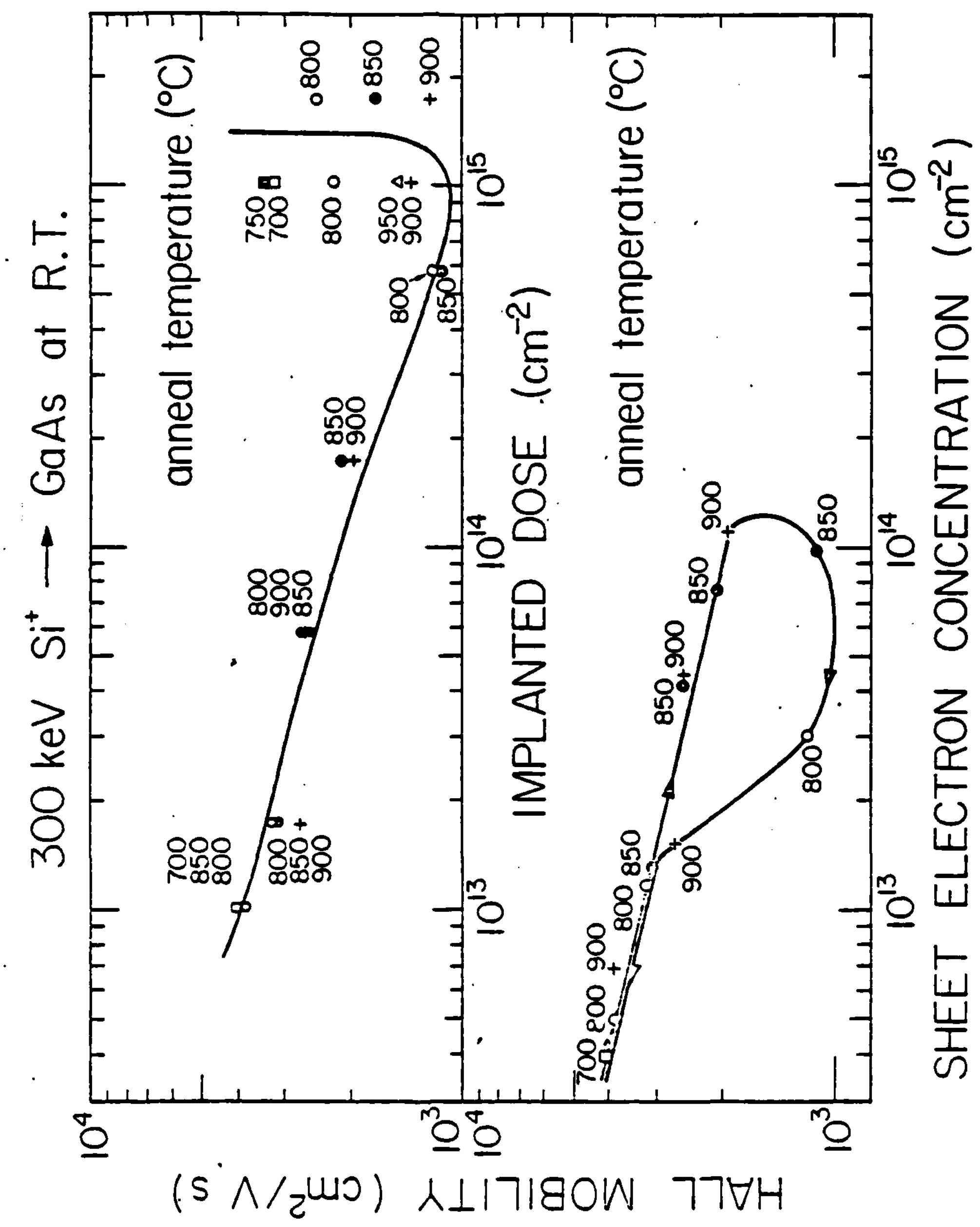

Fig. 3.1-4 Hall mobility vs implanted dose and vs sheet electron concentration.

3.2 Implantation Control (Electronics Research Center)

Precise control of active layer profiles is a critical requirement for large scale integrated circuits. This is particularly true for this GaAs technology since it is specifically aimed at low dynamic switching energies which are achieved mainly through FET devices with low currents and low threshold voltages. The ability to reproduce and control low threshold voltage FETs combined with the reliance on device isolation being provided directly from the semi-insulating substrates place great demands on the material and implantation processes. For these reasons strong emphasis is placed on qualifying and selecting high quality semi-insulating GaAs substrates (see Section 2.2), and on monitoring the implanted active layers after processing.

Three types of implanted layers are commonly used in the SDFL approach: one for the low threshold FET channel; one for the high speed switching diode; and a third type of active layer, which is a combination of the first two, used for the ohmic contact and level shifting diode regions. Primary interest and concern center on the low dose Se implant used for the FET channel since it is by far the most critical and difficult active layer profile to control. The FET pinch-off voltages are designed to be ~1.0 V (the current acceptable range is 0.75 to 1.75 V). It is this low threshold voltage criteria which directly influences the choice of dopant (Se) and energy and dose implantation parameters in order to produce extremely thin (~1500Å) and lightly doped (~10^{17} cm^{-3}) n-type active layer profiles.

A survey of the parallel test chip n^- FET channel profiles for eight GaAs IC lots using four different ingots is presented in Figs. 3.2-1 through 3.2-4. All of these profiles were a result of the implantation of 400 keV selenium ions through the silicon nitride cap (~1000Å) at room temperature for doses in the range from 2.0 to 2.5 x 10^{12} ion cm^{-2}. These parallel test chips are meant to serve as process monitors and are representative of the actual profiles on the IC wafers. For all of these profiles the voltage required to deplete these thin layers to a 10^{16} cm^{-3} carrier concentration level was recorded on the figures. This value is a good relative indication of what the

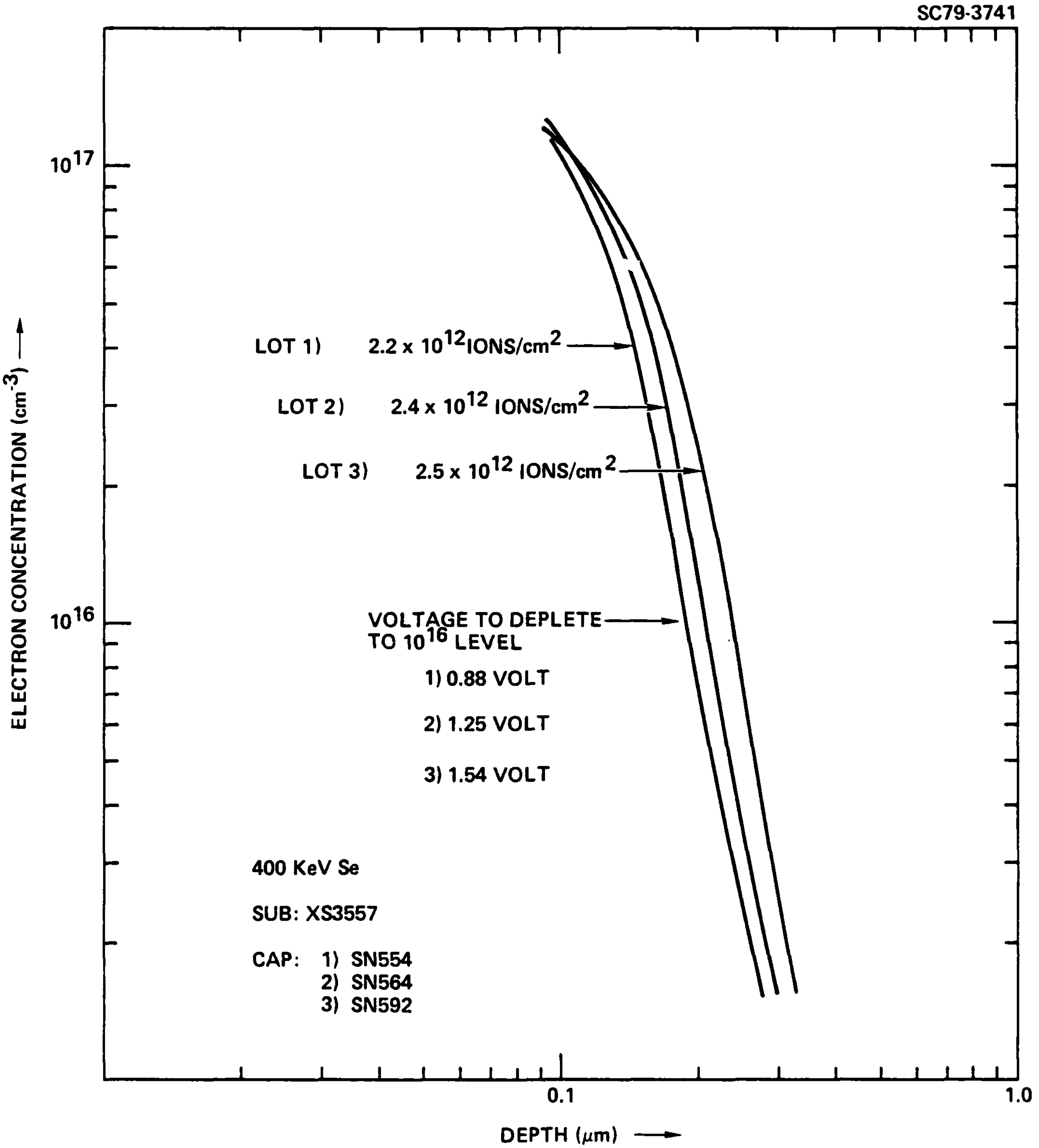

Fig. 3.2-1 Carrier concentration profiles measured on parallel test chips from three IC lots showing the voltages required to deplete these layers to a 10^{16} cm^{-3} level. (from Ref. 1)

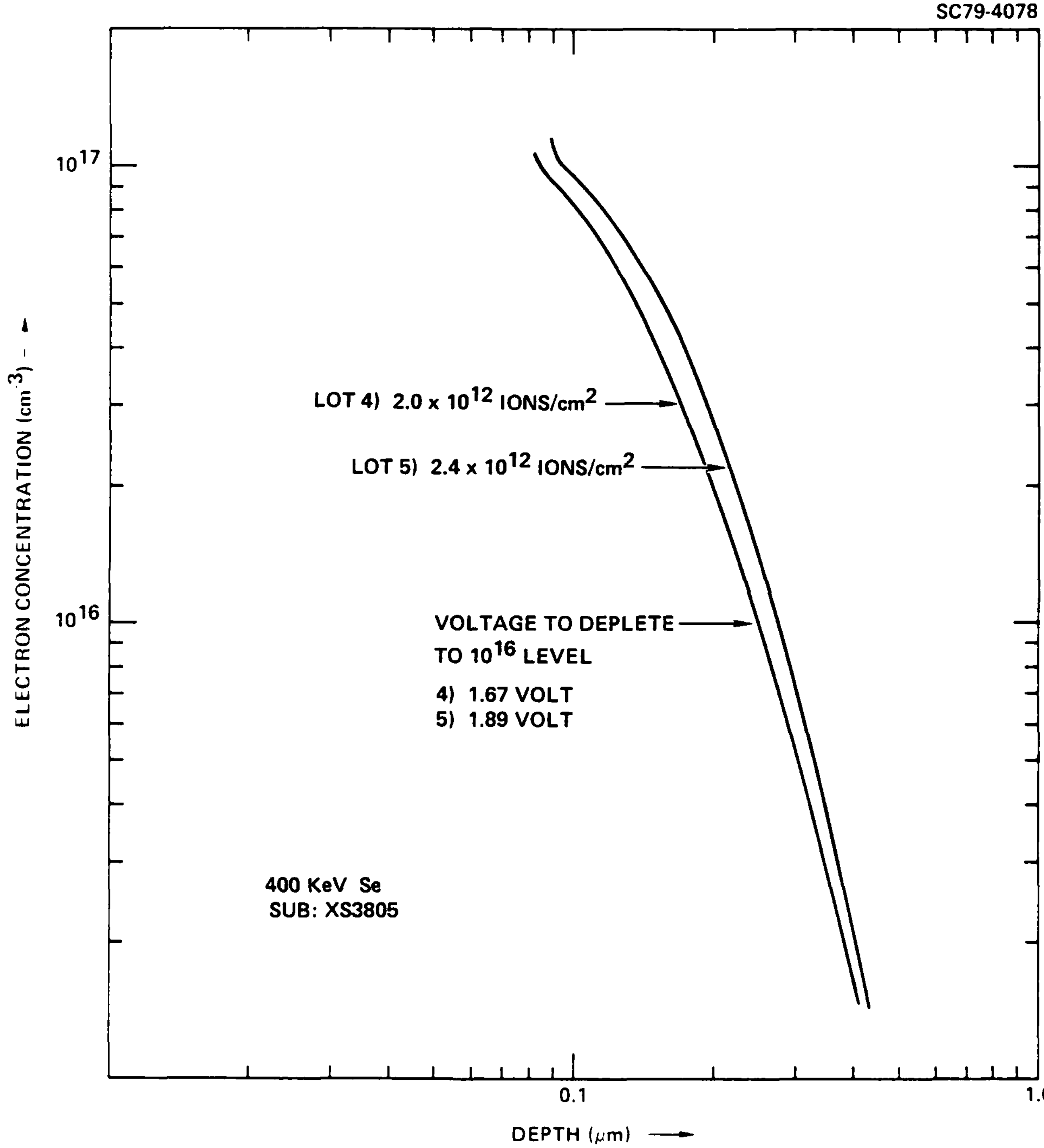

Fig. 3.2-2 Carrier concentration profiles measured on parallel test chips from two IC lots showing the voltages required to deplete these layers to a $10^{16}cm^{-3}$ level.

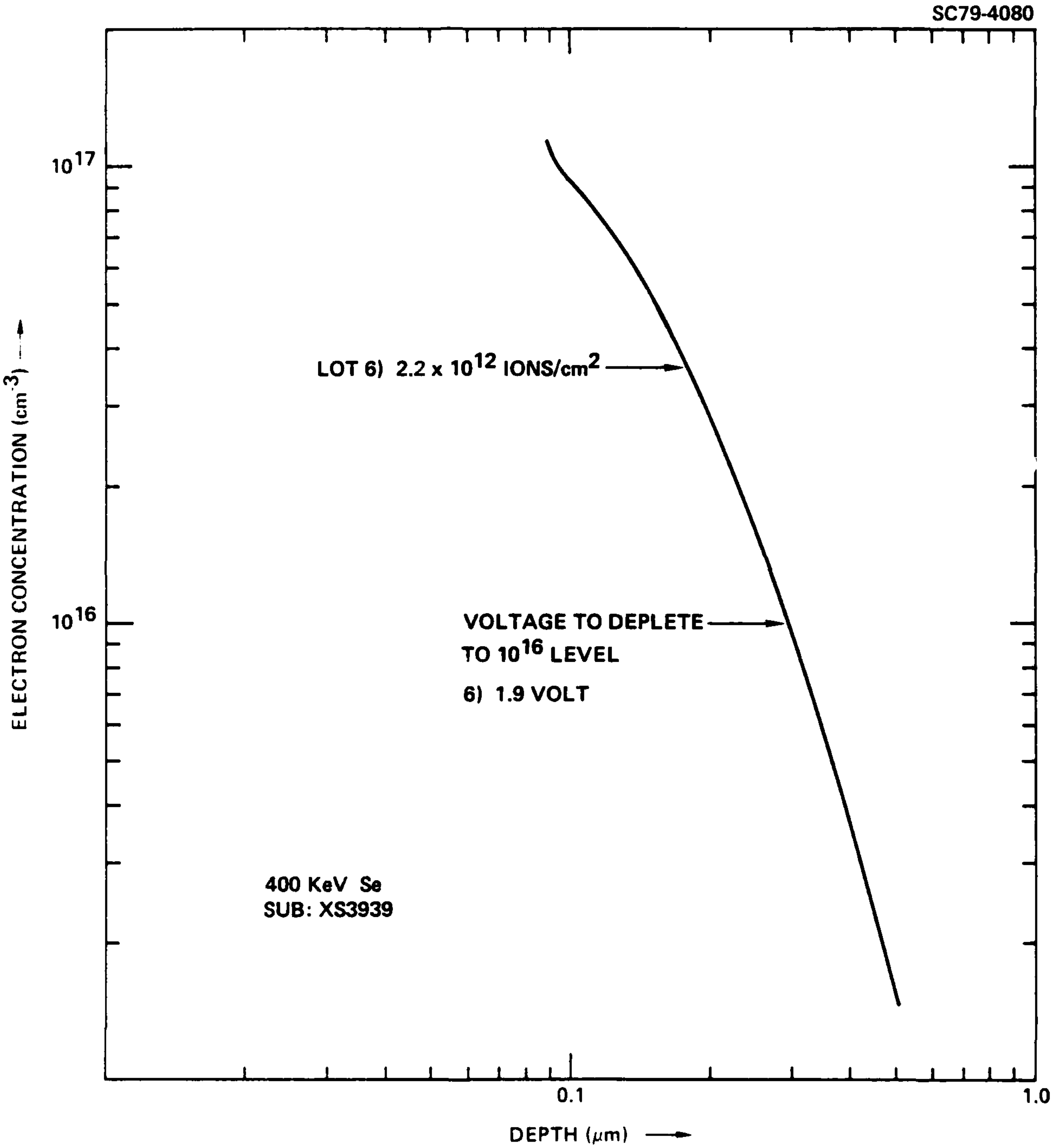

Fig. 3.2-3 Carrier concentration profile measured on a parallel test chip from an IC lot showing the voltage required to deplete this layer to a $10^{16} cm^{-3}$ level.

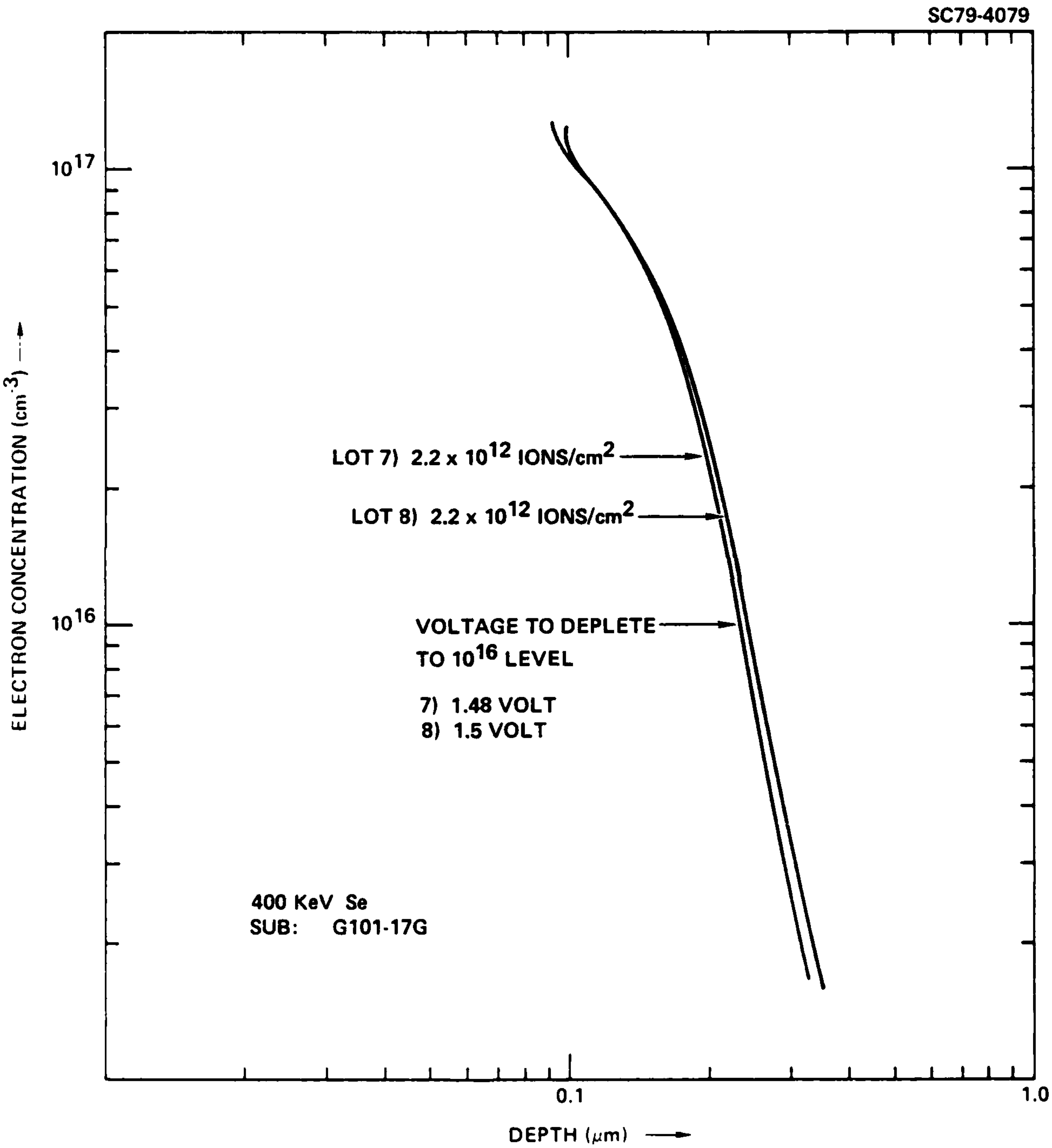

Fig. 3.2-4 Carrier concentration profile measured on a parallel test chip from two IC lots showing the voltages required to deplete these layers to a $10^{16} cm^{-3}$ level.

FET pinch-off voltage should be on devices fabricated with these layers. Some general observations can be deduced from this data. Different GaAs ingots implanted with similar parameters show small variations in the resulting Se profiles. The depletion voltage variations exhibited in these wafers are mainly dependent on the depth of the tail regions in the profiles in the various GaAs ingots. These pinchoff voltage variations can be compensated by adjustments on the doses. Ingot #XS3939 yielded Se profiles with the deepest tail and highest depletion voltage while ingot #XS3557 resulted in the most shallow profiles and lowest voltages. The remaining two ingots, #XS3805 and #G101-17G, yielded Se profiles with depletion voltages generally between the ranges of ingots #XS3939 and #XS3557. All of the peak electron carrier concentrations were just slightly above 10^{17} cm^{-3} showing little variation in the peak doping activation levels.

During the course of numerous semi-insulating GaAs qualification tests, a large amount of data correlating substrate qualification test failures with the appearance of deep tails in the implanted profiles has been accumulated. For the first time the correlation between failure to pass the qualification test and the appearance of deep tails in the implanted profiles and isolation failure has been verified on fabricated wafers. The experiment was conducted on slices from an ingot appraised as marginal during the qualification test because it exhibited satisfactory results only on the tail end. The data shown in Fig. 3.2-5, a plot of semi-insulating substrate leakage currents between 3 µm ohmic contact gaps on a lot of four wafers processed from that ingot, indicate a catastrophic loss of isolation for the slices originating near the front end of the ingot (which failed the qualification test). The wafers with large leakage effects had FET devices with unusually large pinchoff voltages, attributed to deep tails of the implantation profiles. The correspondence between large leakage currents and deep tails was further supported by results from wafer AR2-51, which exhibited correlated variations of both features from one side to the other.

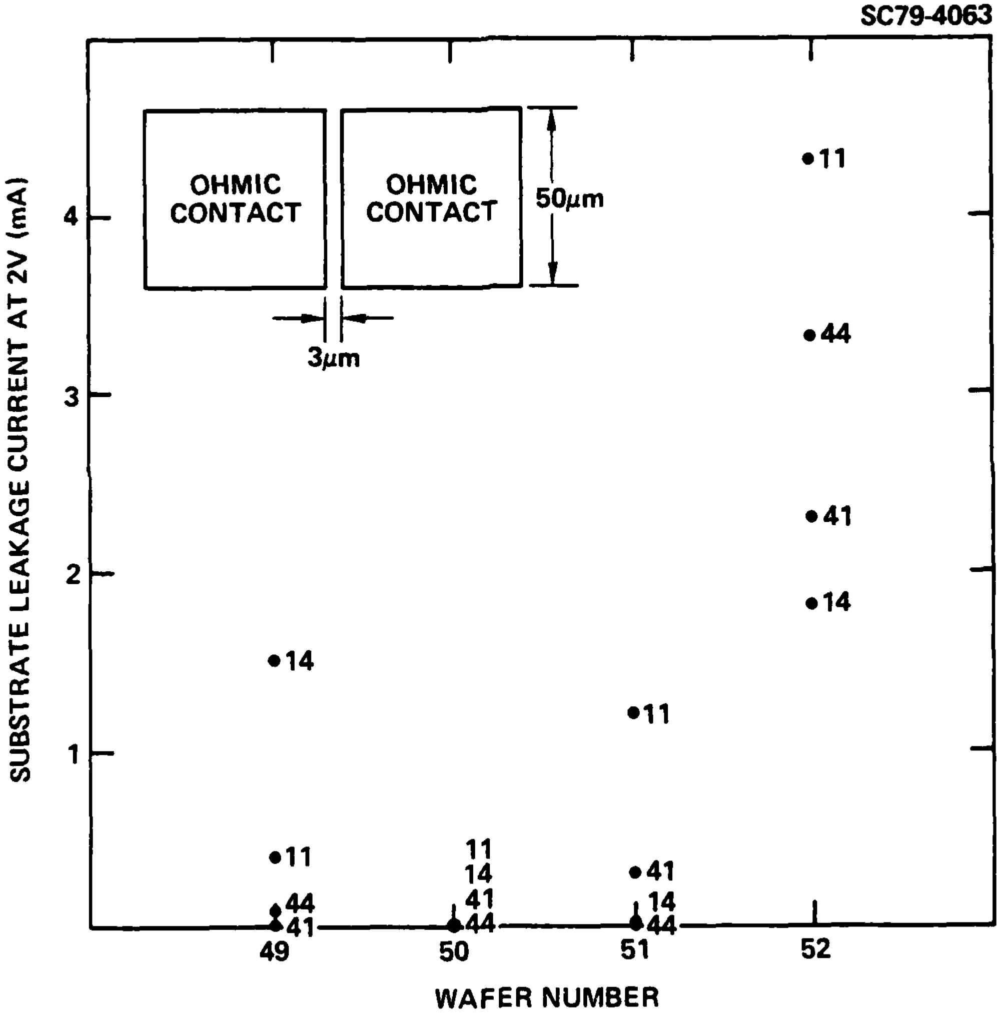

Fig. 3.2-5 Leakage currents measured on four wafers processed from an unqualified substrate. The test pattern dimensions are indicated on the inset.

Use of this particular ingot in the IC process served as a test, providing information on ingots which qualify with marginal success, and verifying that the overall qualification procedures used in this program are adequate to predict the quality and usefulness of a particular GaAs ingot.

3.3 Ohmic Contacts (Electronics Research Center)

Low resistance ohmic contacts in the source and drain of FETs and the cathodes of Schottky barrier diodes are a critical requirement in this GaAs IC process because of emphasis placed on extremely small devices such as 10 μm wide FETs and 1 μm × 2 μm Schottky barrier diodes. Therefore, ohmic contacts are and will continue being a subject of constant analysis and improvement in this program.

Metallurgical ohmic contacts to GaAs are formed by melting a eutectic alloy composed of 88% Au and 12% Ge covered with a thin platinum overlay. A shallow surface layer of GaAs is dissolved during alloying of the AuGe film and immediately regrown upon subsequent cooling. The dopant (Ge) is incorporated in the epitaxially regrown GaAs forming a degenerately doped layer. In this program, a reliable AuGe/Pt ohmic contact system has been developed based on the following conditions: the contact is composed of a 1300Å film of AuGe covered with a 300Å Pt layer; alloying is accomplished using a tube furnace with a hydrogen atmosphere; the samples are exposed to a temperature between 450°C and 465°C and the alloying time from 2 min 15 sec to 2 min 45 sec. The contact metallization thickness, and the time, and the temperature for this process have been optimized.

During the course of this program the quality of the ohmic contacts has continuously improved. The ohmic contacts are probed immediately after the alloying cycle in order to routinely monitor this quality. The test consists of measuring the I-V characteristic of a structure that resembles a FET without gate. The linearity, symmetry and saturation voltage give an empirical indication of the quality of the ohmic contacts produced. However, this routine measurement does not yield the value of the specific ohmic contact

resistance. This is measured after the fabrication process is completed on a test pattern employing gaps of several lengths in order to subtract the channel resistance and calculate the specific ohmic contact resistance, r_c.[8]

Rockwell's multiple localized implant process results in a FET-like device structure more difficult to analyze than the usual single active layer FET structures. For the multiple implant FET structure, the typical metal source to drain varying gap method for measurement of contact resistance yields incorrect results, with r_c values typically far lower than actual figures if the gaps between ohmic contact metal edges are used, ignoring the extra implants. This is illustrated in Fig. 3.3-1 where the dotted line represents the values of contact resistances vs. ohmic contact gap lengths measured between the edges of the ohmic contact metal areas. Note that the dotted line, if extended, will actually cross the negative y-axis indicating negative contact resistance, which is not possible. This happens because, with the more sophisticated FET structure (shown in Fig. 3.3-1), the ohmic metal gap dimensions are irrelevant. Most of the resistance measured for the gaps is due to the n^- region which is considerably shorter than the ohmic metal gaps. The n^-region, formed by a low dose Se implant, has a sheet resistivity of $\rho_s \sim 2500\ \Omega/\square$, while the combined $n^- + n^+$ region under and beyond the edge of the ohmic metal has a sheet resistivity of $\sim 350\ \Omega/\square$. Therefore, a more reliable calculation of ohmic contact specific resistance must use the gaps between the edges of the n^+ regions indicated in the table of Fig. 3.3-1. In addition, lateral diffusion of the n^+ region ~ >2000Å, must be accounted for, yielding the gap dimensions given in the n^+(diff) column of the table of Fig. 3.3-1. Using such dimensions results in a linear dependence of contact resistance on gap length as shown by the solid line of Fig. 3.3-1. The intersect with the y-axis represents the sum of the contact resistance of the two contacts (plus a negligible probe contact resistance of ~2 Ω). The resulting $2R_c$ value is used to determine the actual specific contact resistance calcu lated from the relationship $r_c = \frac{(R_c)^2\ \ell \cdot w}{\rho_s}$ where ℓ and w are the dimensions of the ohmic contact and ρ_s is the sheet resistance under the ohmic contact.[6,7]

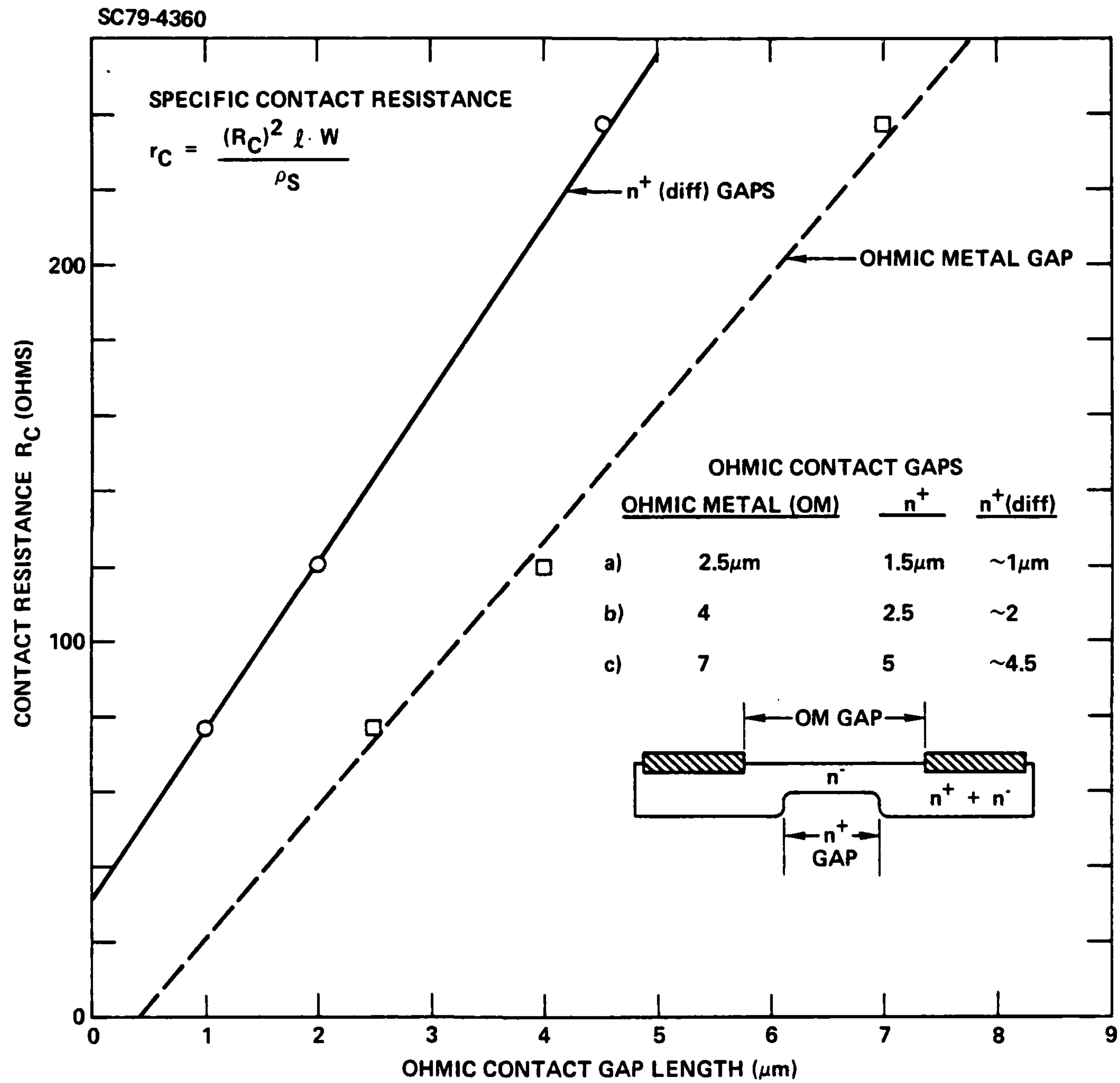

Fig. 3.3-1 Resistance between contacts vs contact separation. The boxes and the dashed line correspond to separations measured between the edges of the ohmic contact metals. The circles and the solid line correspond to separations determined by the length of the n^- layer corrected for the effect of the n^+ layer. The solid line gives correct results.

The ρ_s used in this calculation is obtained from the resistivity measurements on the $n^+ + n^-$ regions of the wafers using Van der Pauw test patterns on the same mask.

During the course of this program specific ohmic contact measurements have been made in order to monitor progress. Figure 3.3-2 shows a sampling of ~20 different GaAs IC chips dating from January 1978 to present. At the start of this program typical values of specific ohmic contact resistance ranged from 2-6 $\times 10^{-5}$ Ω-cm^2. By continuously improving and optimizing the ohmic contact process, the specific ohmic contact resistance has gradually been reduced. The current ohmic contact process always results in values less than 10^{-5} Ω-cm^2 and typically in the range of 2-6 $\times 10^{-6}$ Ω-cm^2.

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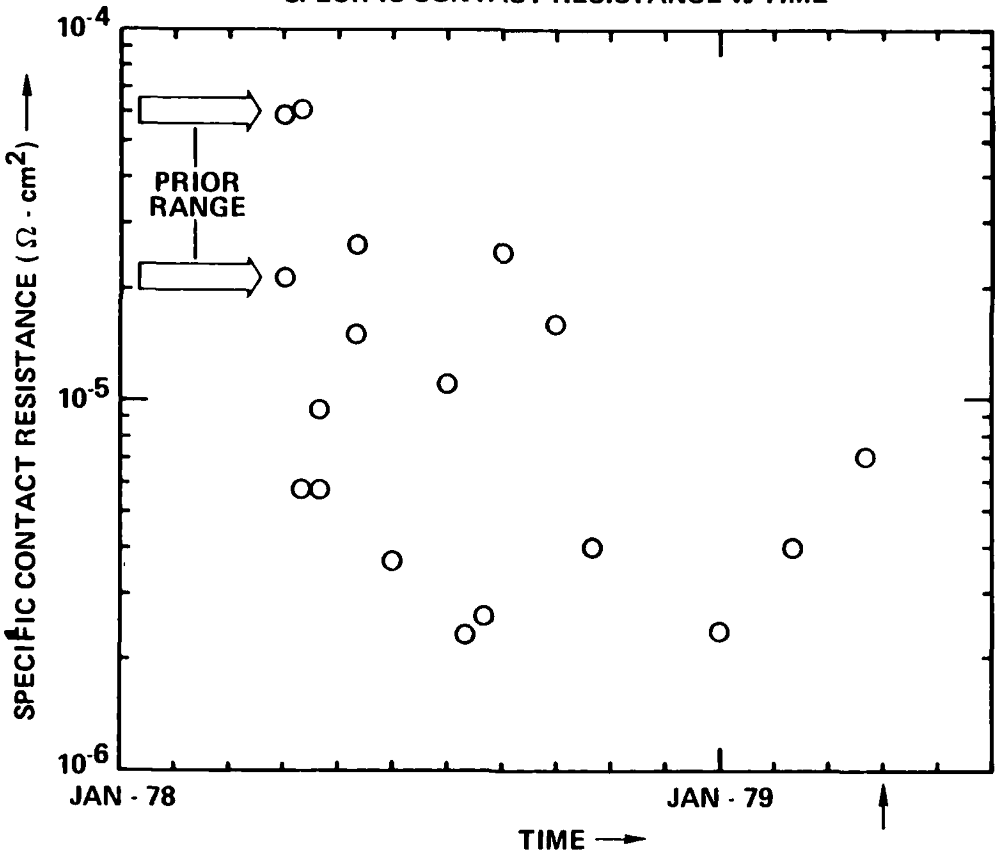

Fig. 3.3-2 Evolution of specific contact resistance measured on processed wafers showing steady improvement over the contract period.

4.0 CIRCUIT PERFORMANCE

Circuit and device testing is a critical activity within the program. Every wafer is currently tested before and after the second layer metallization process using the automatic measurement system described in previous reports.[1] The characteristics of diodes and FETs are mapped over the wafer. Acquisition of C-V data using the automatic probe station has recently been implemented. This test will be incorporated in the normal procedure for wafer evaluation shortly, as soon as the programs required for the analysis of the data and calculation of the doping profiles are completed. Another automatic measurement has been incorporated. It consists of correlating the saturation current for neighboring FETs and active loads in the T2 test pattern in order to determine whether the short range fluctuations of device parameters are smaller than the long range variation. Results from these tests will be presented and discussed in Section 4.1. Long chains of gates were tested. Results showing high yield of fully working 98 and 84 gates will also be presented in Section 4.1.

Tests of MSI circuits have continued. The 8:1 data multiplexer and the 1:8 data demultiplexer have both been evaluated at clock frequencies of approximately 1.1 GHz. The ÷8 circuits on the AR2 mask set have been operated at frequencies as high as 1.9 GHz. These results will be presented and discussed in Section 4.2.

4.1. Automatic Measurements - Low Speed Testing (Electronics Research Center)

Statistical results on device characteristics (FETs and diodes) are obtained from a large number of devices (72 in AR2) uniformly distributed over the wafer. The separation between devices is on the order of 1.5 mm. Data on average values and standard deviations for the parameters of these devices (such as pinchoff voltage and saturation currents) are calculated by the automatic measurement system. A question that remains to be addressed is whether

devices located much closer to each other, at distances on the order of 100 μm or less (circuit scale), would exhibit the same or lower standard deviations of device parameters. A full answer to this question will be obtained from the new mask set, AR3, which contains dense arrays of FETs and diodes. However, some insight into the short range correlation of device parameters can be obtained from the mask set AR2 currently under test.

Figure 4.1-1 shows the test cell, T1/T2, which is uniformly distributed over the mask such that there are 72 such cells over a wafer. This figure was reproduced from the previous final report.[1] T2 contains the FETs and diodes normally tested by the automatic measurement system. Counting one FET and two active loads in the gate, there are altogether five FET devices in T2. Each one of these devices can be probed separately from the others. This measurement can be easily implemented with the automatic measurement system which has a cross point relay matrix capable of sequentially connecting each one of the devices to the measurement units. S ce some of the devices are active loads, the FETs are all treated as active loads, their gates being grounded for the measurement. Although from the active load characteristics it is possible to calculate only saturation currents, the statistical data accumulated over many wafers have shown a very strong correlation between the pinchoff voltage and the saturation current for the FETs. Therefore, the relative values of saturation currents normalized for the width of the active loads can be assumed to reflect the relative values of the pinchoff voltages.

A test consisting of sequentially measuring the I-V characteristics of each one of the five active loads (or FETs treated as active loads) in T2 has been implemented and applied to all the wafers recently processed. The results from these measurements can be best discussed by comparing data from two wafers, one exhibiting very poor long range uniformity in device parameters, and the other having excellent long range uniformity.

Figure 4.1-2 corresponds to the first case, which is atypical because the data were taken from an experimental wafer fabricated on a substrate that did not pass the qualification tests. This wafer exhibits variation of its

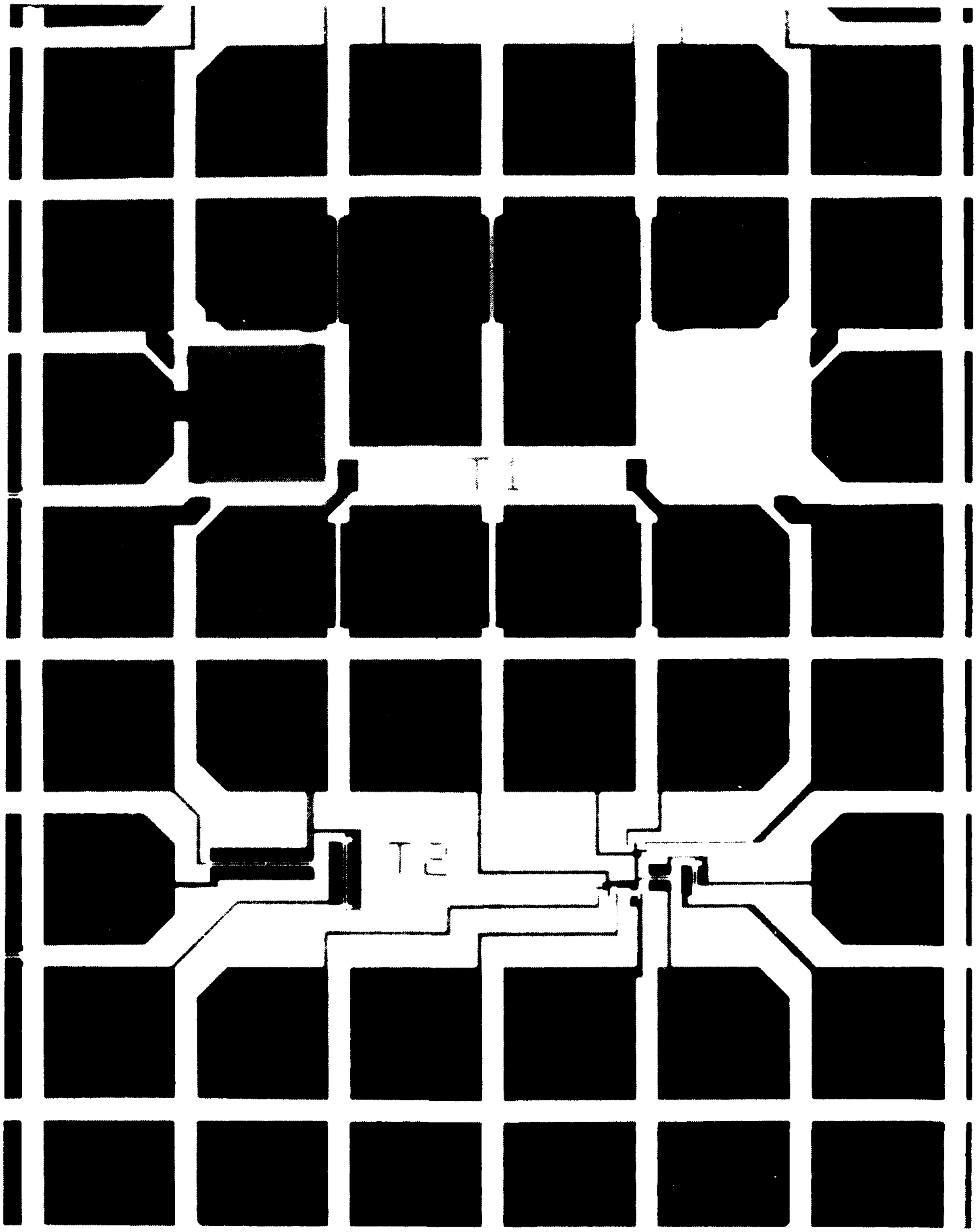

Fig. 4.1-1 Test pattern utilized for comparing saturation currents of neighboring FET devices (from Ref. 1).

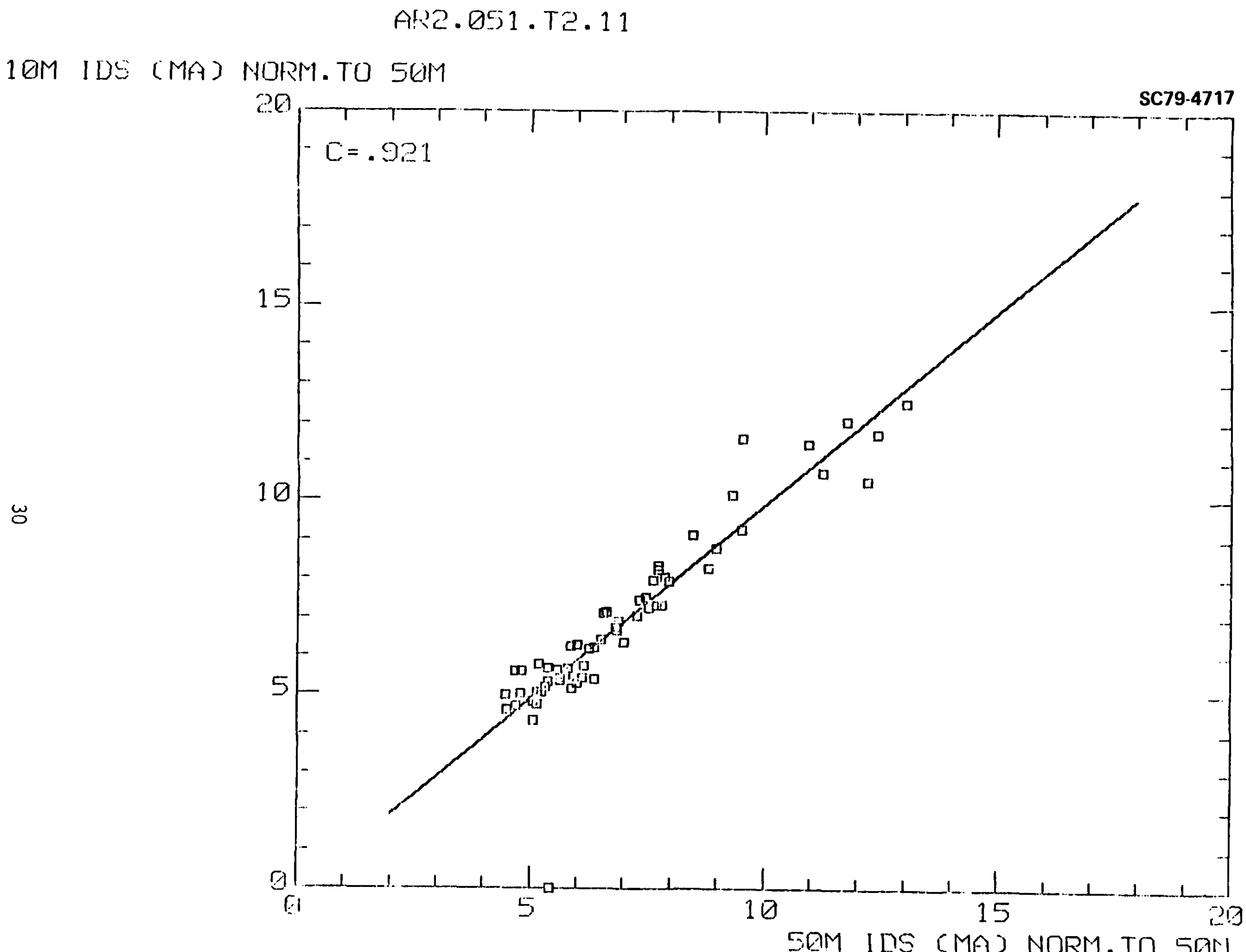

Fig. 4.1-2 Saturation currents of 10μm wide FETs (normalized to 50μm) vs the saturation currents of their neighboring 50μm wide FETs for a wafer exhibiting exceptionally bad long range nonuniformity. The corre-

substrate isolation characteristics from one side to the other. Along with this variation, the wafer exhibits a distorted implantation profile on the side with poor isolation, resulting in a very large spread in device saturation currents. Figure 4.1-2 plots the saturation current through the 10 µm FET in the T2 gate (normalized to 50 µm width) against the saturation current of the 50 µm wide FET (the one on the left side of T2, Figure 4.1-1) for each one of the T2 test cells over the wafer. The large spread in saturation current values from one side of the wafer to the other is reflected by the large scatter of the points both in the horizontal and vertical direction. However, there is very strong correlation between the points. Where the current for one device is low the current for the other device in the same cell is also low. The same strong correlation applies to any pair of devices within the T2 cell. This figure highlights the observation that when there is a uniform trend of variation of FET characteristics over the wafer, no matter how large, the differences between the values of parameters for neighboring devices are much smaller.

Figure 4.1-3 shows a plot of the same parameters displayed in Fig. 4.1-2, but for the opposite case in terms of long range uniformity. This wafer shows excellent uniformity of FET parameters, the saturation current for the 50 µm wide FETs exhibiting a standard deviation of only 0.63 mA, representing only 9.8% of the average value. According to the wafer map the variations are random. Fig. 4.1-3 shows that in this case there is virtually no correlation between the values of the current through the 50 µm FETs and the 10 µm FETs. Therefore, the short range fluctuations of saturation currents are as large as the long range fluctuations.

The conclusion, reached from observations of a variety of wafers and highlighted in Figs. 4.1-2 and 4.1-3, is that the short range variations of saturation currents on most of the wafers are of the same order as the long range variations observed on the wafers showing the best uniformity. This result is quite satisfactory since it demonstrates the capability of obtaining excellent uniformity on a wafer. The remaining fluctuations, on the order of

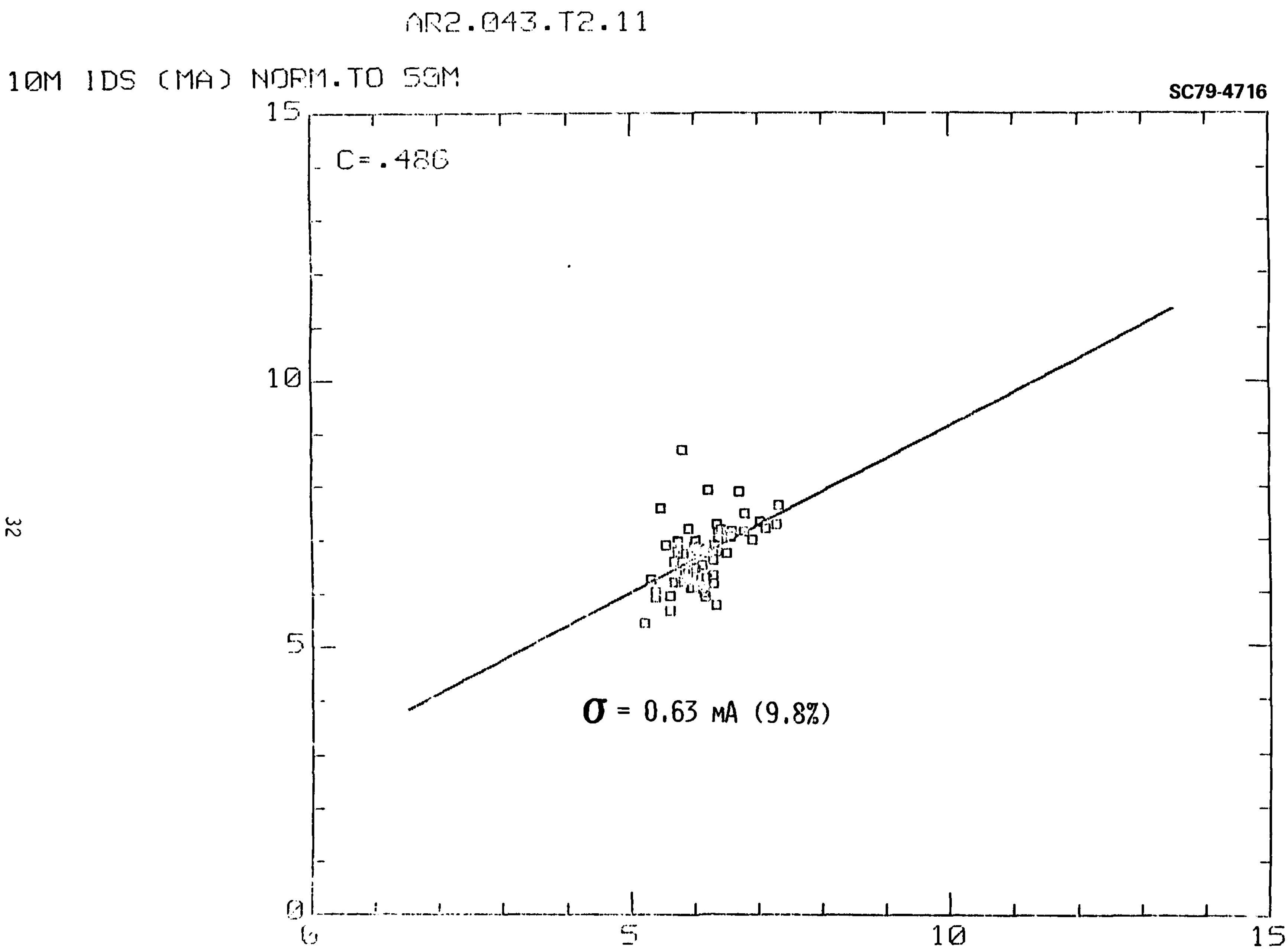

Fig. 4.1-3 Saturation currents of 10μm wide FETs (normalized to 50μm) vs the saturation currents of their neighboring 50μm FETs for a wafer exhibiting good long range uniformity. The lack of correlation indicates that the short range variations are approximately equal

10% to 15% of the average value at most, must be viewed as totally random over the wafer and, therefore, independent of the distance between devices.

Long chains of gates were incorporated in the design of mask set AR2 as a tool to easily gain insight into the yield capability of the process. Figures 4.1-4 and 4.1-5 show SEM micrographs of such long chains containing 84 gates with 10 μm wide FETs, and 98 gates with 5 μm wide FETs, respectively. As shown in the figures, each chain has a single input from which the signal propagates through all the gates and reaches the output. Each gate acts as an inverter. There are intermediate taps to monitor the operation of portions of the chains. No buffering circuits for high speed tests were designed. The goal was to test circuits involving a large number of gates at low speed with a minimum amount of instrumentation. Only the instruments used for single gate tests were employed, an oscilloscope, a signal generator, and a dual power supply. Figure 4.1-6 shows examples of output transfer characteristics for an 84 and a 98 gate chain, respectively. The transfer characteristics are displayed in the same manner as gate transfer characteristics, output voltage vs. input voltage. The oscilloscope waveforms show no inversion because there is an even number of gates causing an even number of signal inversions. Note the sharpness of the transition from low to high, due to the fact that the gain of the chain is the product of the gains of many gates.

The test of long chains was made on one wafer only. Results were very encouraging in terms of yield. As shown in Table 4.1-1, out of 8 chains of 98 gates (the other four could not be probed due to restrictions from probe configuration), four chains (50%) worked fully. One more chain worked after 50 gates, and all the other chains worked up to 20 gates at least. As indicated in the table, the yield for the chains of 84 gates was slightly lower, with 4 out of 12 gates, 33%, working fully.

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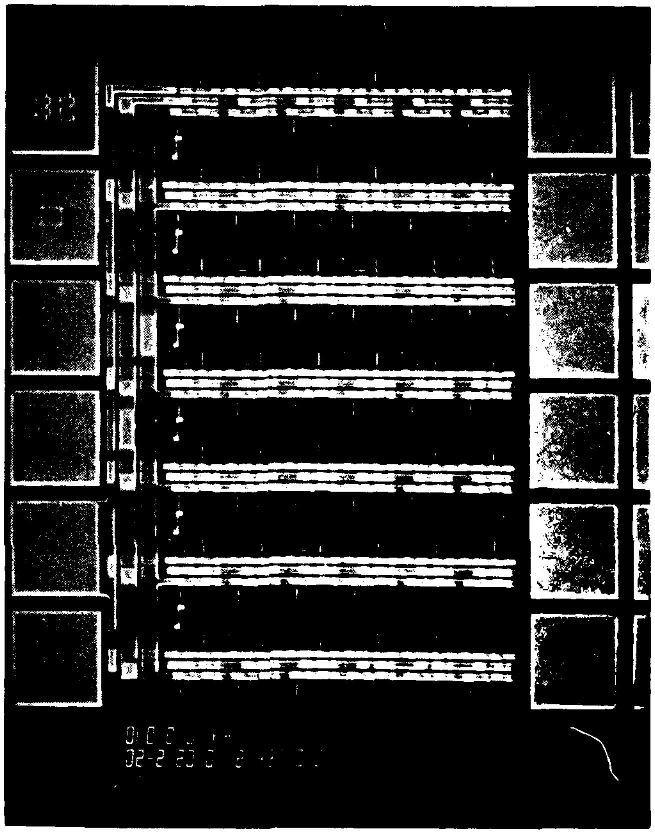

Fig. 4.1-4 Scanning electron micrograph of a chain of 84 gates having 10μm wide, 1μm gate, FETs.

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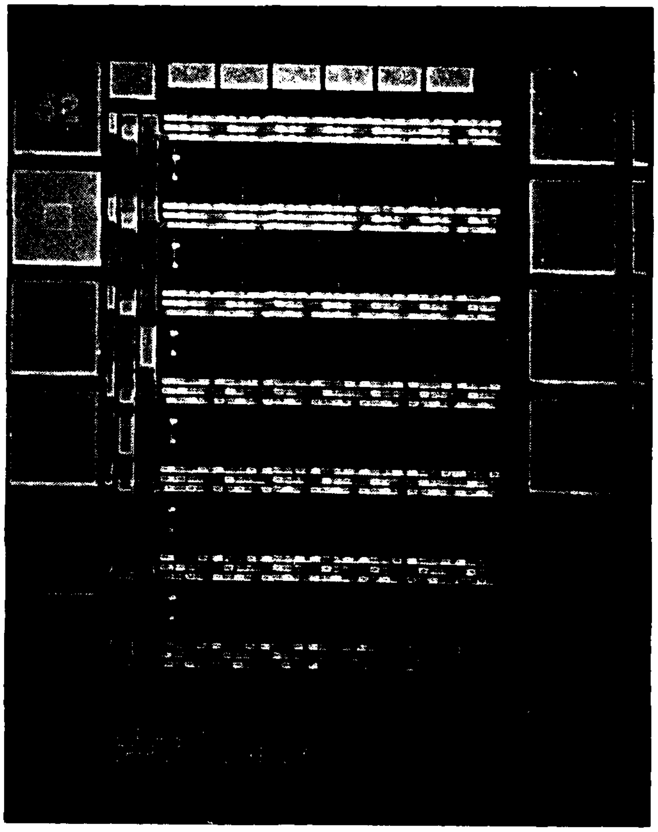

Fig. 4.1-5 Scanning electron micrograph of a chain of 98 gates having 5μm wide, 1μm gate, FETs.

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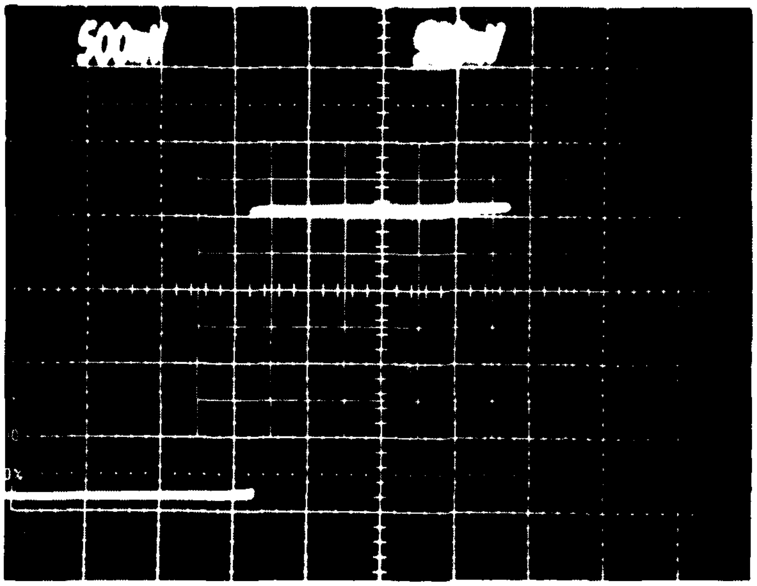
WAFER AR2-47
CHIP 63

V_{OUT}

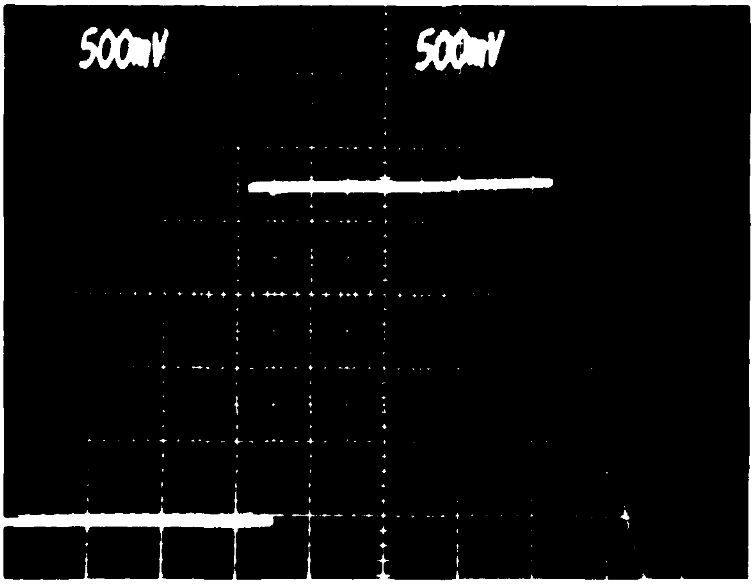


V_{IN}

CHAIN OF 84 GATES
10μm FETs

$V_{dd} = 3.7\ V$
$V_{ss} = -1.6\ V$

V_{OUT}



V_{IN}

CHAIN OF 98 GATES
5μm FETs

$V_{dd} = 3.7\ V$
$V_{ss} = -1.9\ V$

Fig. 4.1-6 Transfer characteristics (V_{OUT} vs V_{IN}) for chains of gates connected as inverters.

Table 4.1-1. Yield of Long Chains - Wafer AR2-47

Chain of 98 Gates (5 μm FETs)			
	Out of 8:		
		Work fully:	4 (50%)
		Work more than 50 gates:	5 (65%)
		Work more than 20 gates:	8 (100%)
Chain of 84 Gates (10 μm FETs)			
	Out of 12	Work fully:	4 (33%)
		Work more than 42 gates:	6 (50%)
		Work more than 7 gates:	8 (67%)

4.2 High Speed Testing (Electronics Research Center)

In this section, a description of high speed evaluation methods used to evaluate the ARPA MSI demonstration circuits will be presented. All dynamic evaluations have been carried out at the wafer probe level in order to effectively utilize the multiple chip and circuit format employed on the ARPA mask sets (See Section 5.0) and to minimize high speed interfacing problems. Performance obtained from the AR2 MSI demonstration circuits will be reported, with considerable improvements in operating clock frequency being obtained since the last reporting period.[2] Divide-by-8 binary ripple counters have now performed up to 1.9 GHz, and the multiplexer/demultiplexer circuits have been demonstrated up to 1.1 GHz.

The evaluation of the MSI circuits was performed on a high speed probe station. Tungsten probes, made by Rucker and Kolls, individually positioned by a 3-axis manipulator provided all connections to the circuits. An example of a typical measurement configuration is shown in Fig. 4.2-1. The

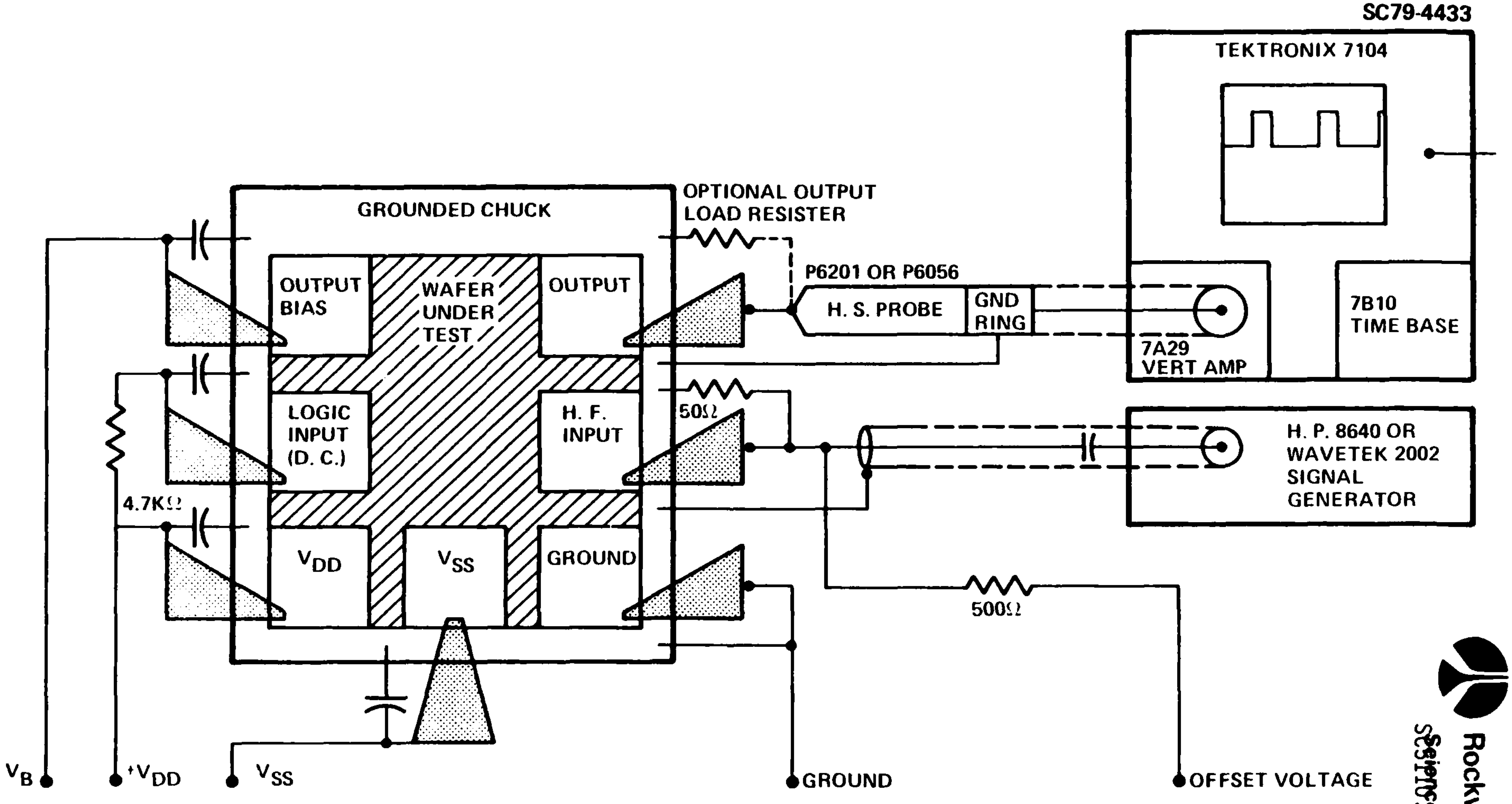


Fig. 4.2-1 Block diagram of high speed test circuits.

high frequency input probes are driven through a 50 Ω coaxial cable connected as closely as possible to the probe terminal. A 50 Ω load terminates the cable. The shields are connected to the chuck of the High Speed Probe Station (HSPS) in order to establish a ground reference plane as close to the wafer and probes as possible. There is also a 500 Ω resistor through which a DC offset voltage is applied so that a sine wave generator can be utilized as a clock source. Clock signals were provided by a Tektronix PG502 pulse generator up to 250 GHz. Between 250 and 1500 MHz, sine wave generators (HP8640B and Wavetek 2002) were used as signal sources.

Output probes drive either a 50 Ω coaxial line or are terminated with a load resistor on the probe. In the latter case, high impedance passive or buffered Tektronix probes, with 3.5 GHz and 0.9 GHz bandwidths, respectively, are used to monitor the output voltage. Output waveforms are monitored using either a sampling oscilloscope (Tektronix 7512) or a high speed, 1 GHz, real time oscilloscope (Tektronix 7104).

While performing high speed tests, as the input frequency was raised, it was not uncommon to observe dropouts where the output would be lost for a small frequency span. This is attributable to a substantial length of unterminated line at the probe tip (approximately one inch) which can cause reflections that vary the amplitude and shape of the input signal. A superior type of probe, built on a hybrid substrate, is now under development on a Rockwell IR&D program and will be applied to the testing of these circuits when available. These probes will also alleviate the difficulty of having an insufficient number of probes to perform certain tests completely. With the present configuration there are eight manipulators, and two are typically equipped with double probes for testing larger circuits; on the multiplexer circuit there are 18 logic inputs, as well as outputs and power supply lines also requiring probes (see Fig. 4.2-9). With the new probes each pad will have one dedicated probe and therefore the probes will not have to be moved while a circuit is under test.

During the past quarter, high speed evaluation of AR2 wafers has concentrated on three circuits. The first circuit is a 3-stage ripple divider, which utilizes D type flip-flops to perform the dividing function for each stage. The second circuit is a high speed 8-line to 1-line data multiplexer which has select lines controlled by a 3-stage synchronous counter, also included in the circuit. This utilizes NOR gates and D type flip-flops to perform its function. In the third circuit there is a 1-line to 8-line data demultiplexer circuit which is similar in design to the multiplexer. The following paragraphs will present high speed data obtained from these three circuits.

A three stage binary ripple counter is located in subchips CD25 and CE55 of mask set AR2. A SEM (Scanning Electron Microscope) photograph of this circuit is shown in Fig. 4.2-2. A corresponding schematic is shown in Fig. 4.2-3. This circuit consists of three D type flip-flops (DFF), where the input to the first flip-flop is supplied from an external clock. Each D flip-flop is "T" connected, i.e., the D input is internally connected to the $\bar{Q}$ output as shown in Fig. 4.2-4. This feedback connection provides a divide-by-2 characteristic. Therefore, this three stage circuit is useful as a ÷2/4/8 frequency divider or ripple counter and could readily be applied for use as a prescaler. Logic simulation indicates that this DFF T-connected divider should function properly up to a maximum clock frequency of 1/4.85 τ_D, where τ_D is the worst case gate propagation delay.

All of the outputs from the divider are connected to buffers, which are connected to probe pads through larger FETs used in source follower configurations. The drains of these FETs are commonly biased through a separate probe because V_B should have a slightly higher voltage than the V_{DD} used for the logic portion of the circuit. Also, meaningful power measurements can be made, since the power dissipation of the logic segment of the circuitry can be the power dissipation of the source follower outputs.

Measurements of the high speed performance of these dividers are summarized in the next three figures. Figure 4.2-5 shows the relationship of the

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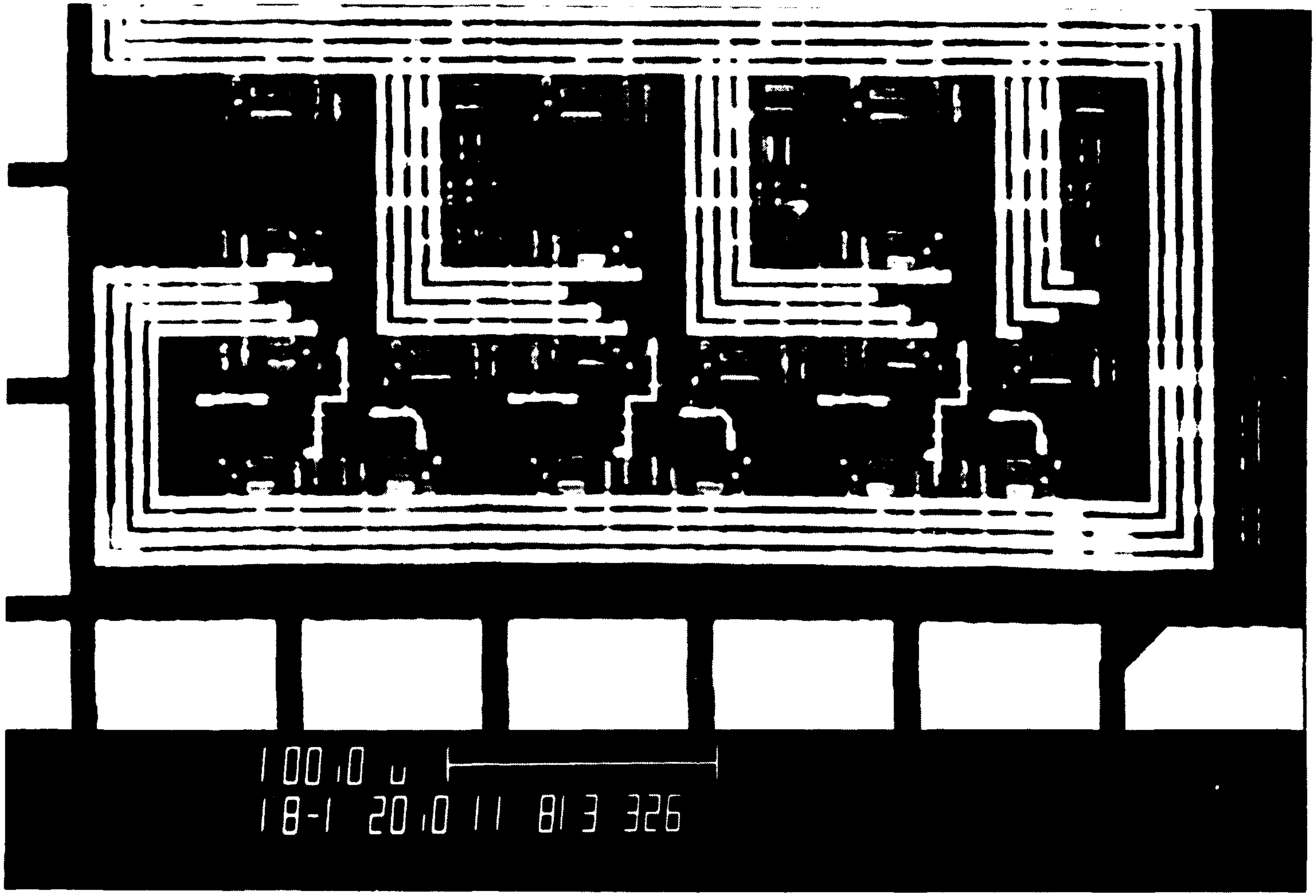

Fig. 4.2-2 SEM photograph of binary ripple divider (CD25).

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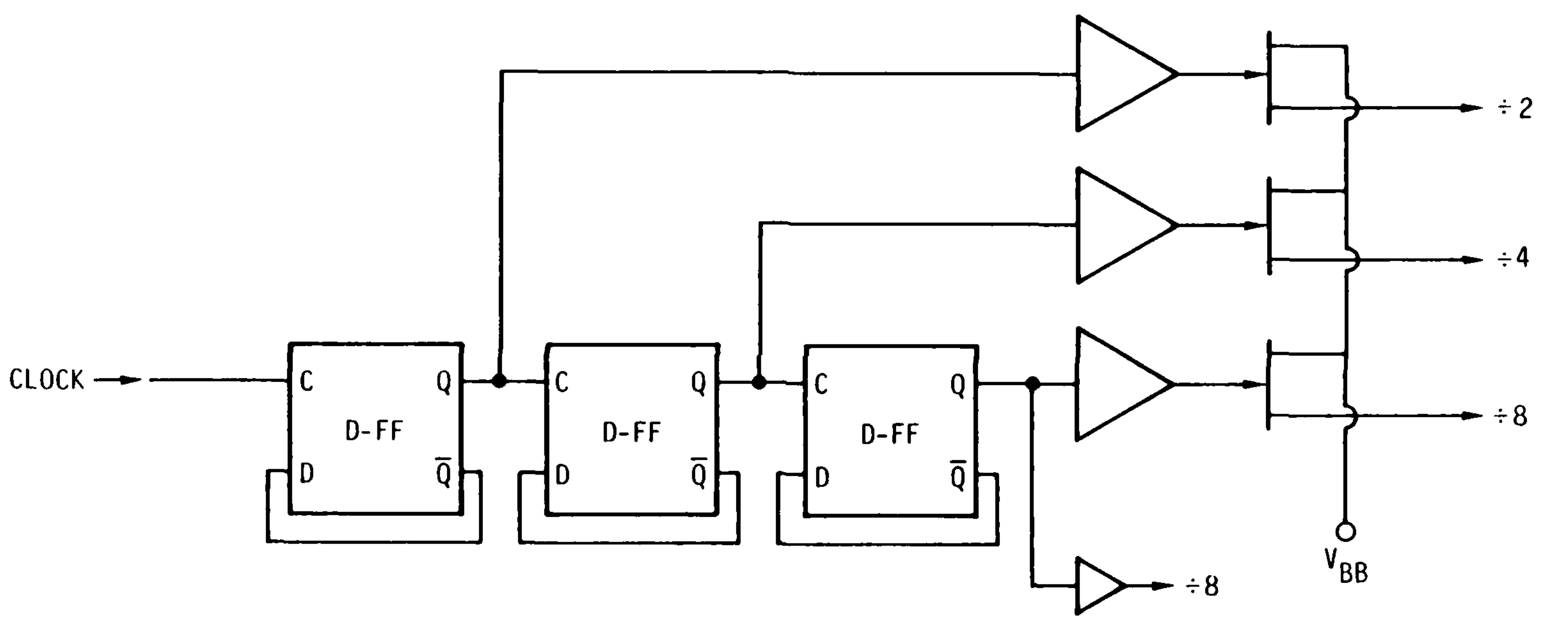

Fig. 4.2-3 Schematic diagram of a 3-stage D flip-flop binary ripple divider.

NOR-IMPLEMENTED TYPE D FLIP FLOP
(SHOWN T-CONNECTED FOR ÷2)

SC78-2590

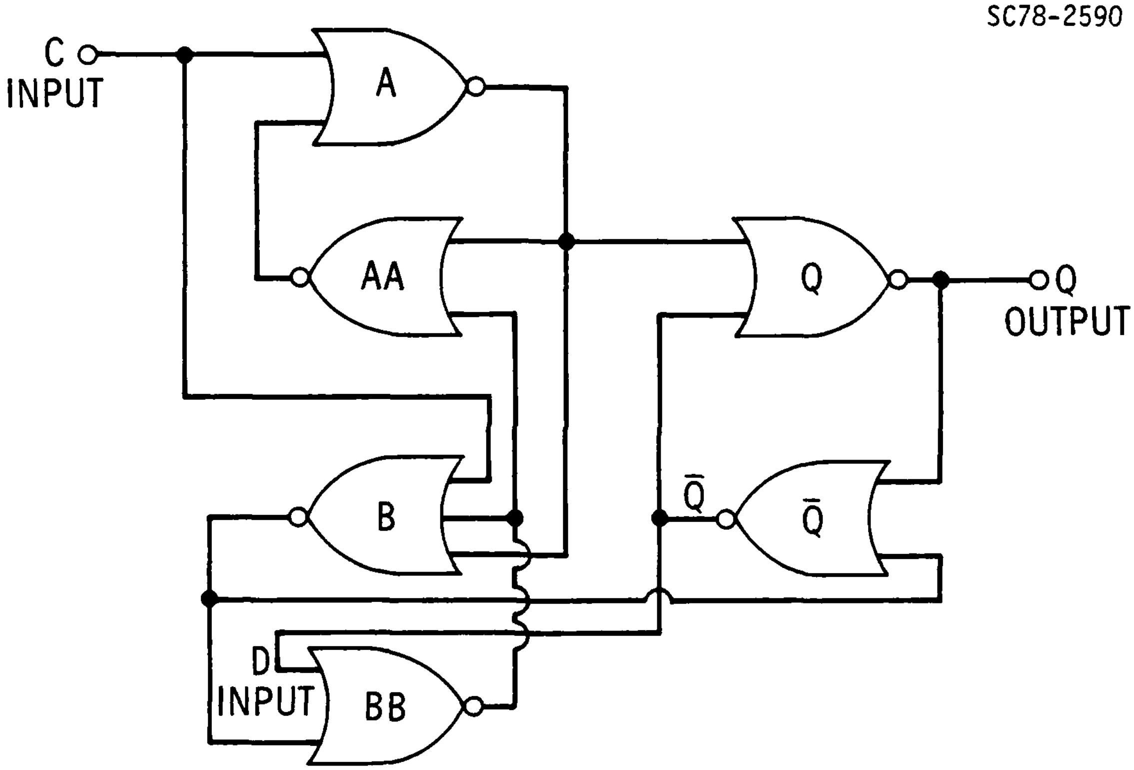

Fig. 4.2-4 Schematic diagram of a T-connected D flip-flop.

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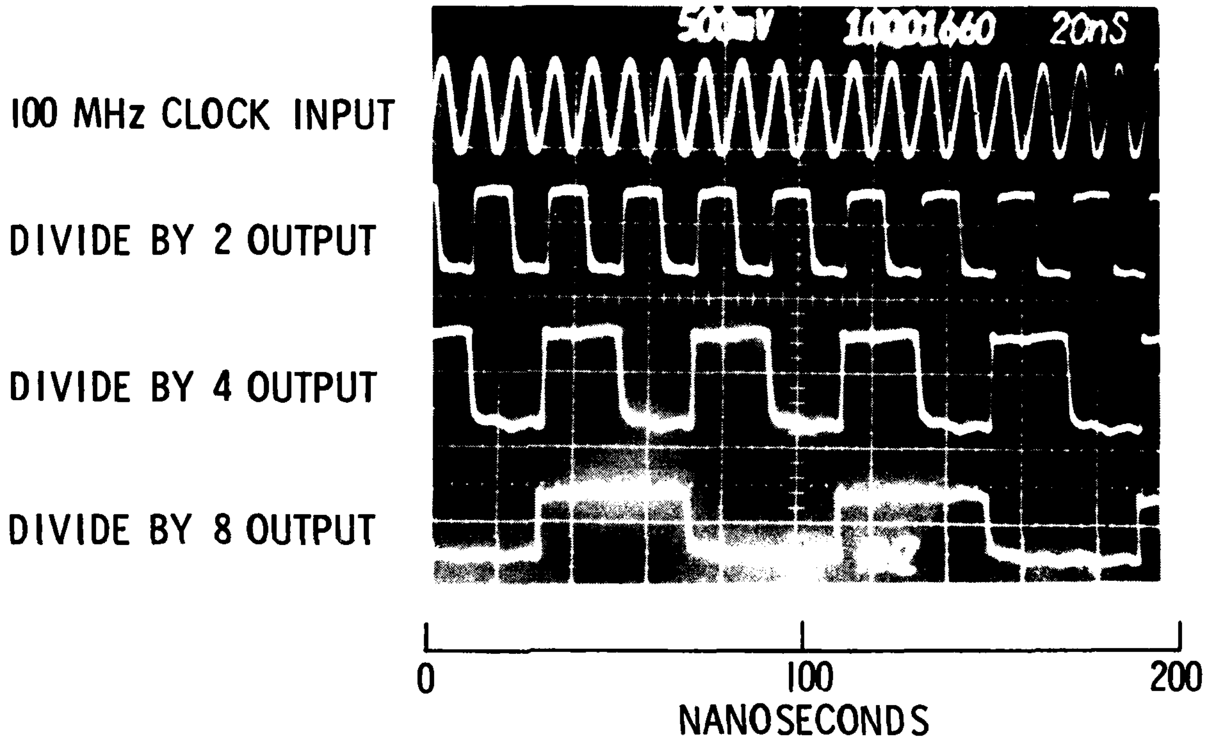


3 STAGE D FLIP-FLOP DIVIDER OPERATION AT 100 MHz CLOCK FREQUENCY

Fig. 4.2-5 3 stage D flip-flop divider operation at 100 MHz clock frequency.

input clock to the three outputs. This photo was taken with an input clock frequency of 100 MHz. Note that the frequency of each subsequent output is half that of the output immediately preceding it. Figures 4.2-6 and 4.2-7 show the ÷8 output of a divider at clock input frequencies of 1.38 GHz and 1.9 GHz, respectively. The 1.9 GHz input frequency marks the fastest input clock which yielded a proper output on any MSI circuit tested to date. This corresponds to an equivalent propagation delay of 110 ps/gate, in reasonable agreement with 10 μm NOR ring oscillator measurements. This represents a considerable improvement over the previously reported (Ref. 1, Sec.7.2) DFF divider results which had a maximum clock frequency of 850 MHz. Since the DFF chain contains gates with fanouts of 2 to 4 and is a sequential logic circuit, this high speed performance shows that the SDFL circuit approach is not limited to low speeds or low fanouts. Total power dissipation of the 3-stage dividers ranged from 45 to 145 mW, depending on operating bias conditions.

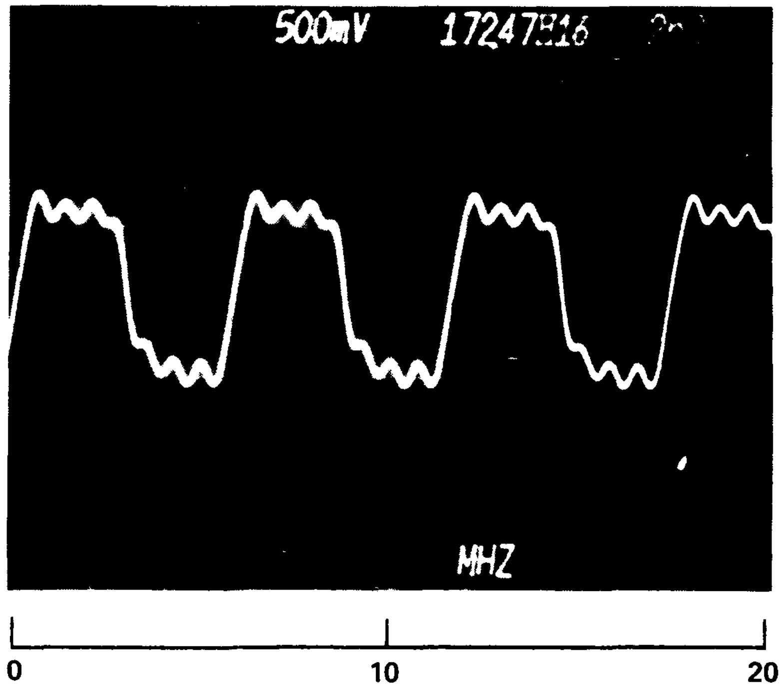
The dynamic switching energy for a standard 10 μm SDFL NOR gate was calculated from the measured divider data, assuming that the maximum clock frequency attained represented the minimum propagation delay of $\tau_D = 1/(4.85\ fc)$ determined by the logic simulation of the DFF. The dynamic switching energy ranged from 0.25 to 0.44 pJ/gate for these circuits.

Good yield of working divider circuits has been observed. For example, on one wafer, AR2-48, out of 20 divider circuits tested, eight were found to be fully functional well above 1.2 GHz, seven others were either fully functional at <1 GHz or partially functional at >1 GHz (i.e., ÷2 and ÷4 output but no ÷8 output) and two functioned partially before failing during test.

An 8-input data multiplexer is located in subchips CD11 and CD33 of mask set AR2. This circuit repeatedly selects 1 out of the 8 inputs during each full clock cycle and connects it to the output port. This type of circuit is useful as a high speed parallel to serial converter which could be used for gigabit data transmission.

SC79-4052

DIVIDE BY 8
OUTPUT



3 STAGE D FLIP FLOP DIVIDER OPERATION AT 1.38 GHz CLOCK

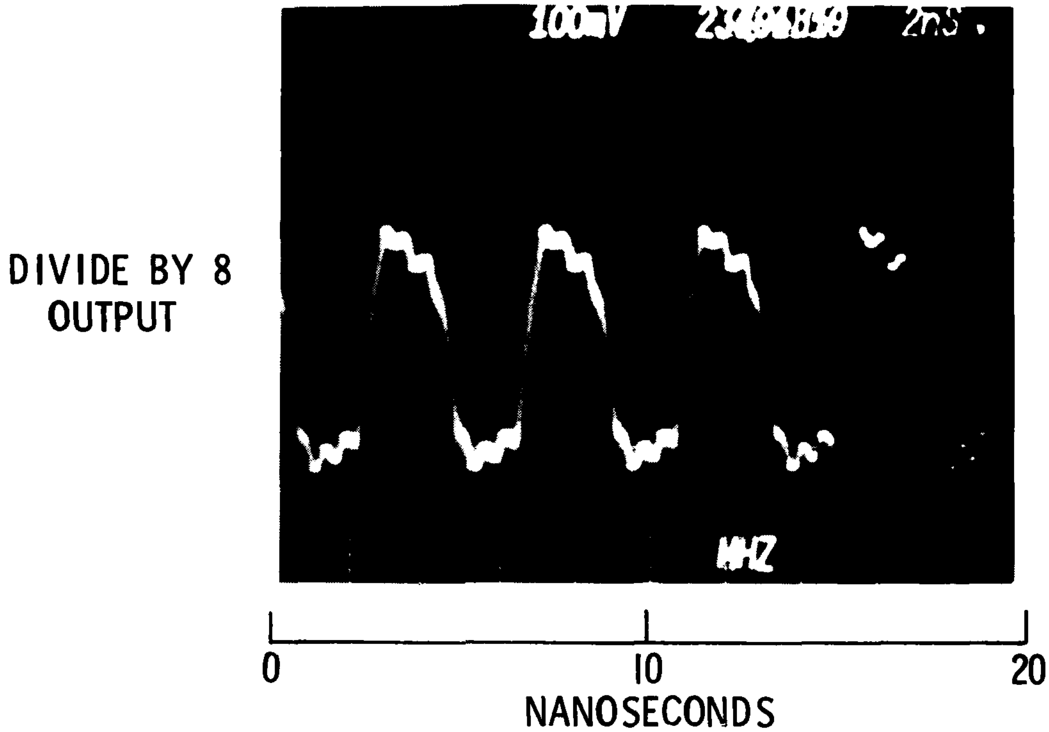
POWER DISSIPATION = 78 mw

DYNAMIC SWITCHING ENERGY = 0.33pJ/GATE

PROPAGATION DELAY = 149 ps/GATE

Fig. 4.2-6 3 stage D flip-flop divider operation at 1.38 GHz clock.

SC79-4054



3 STAGE D FLIP-FLOP DIVIDER OPERATION AT 1.9 GHz CLOCK

POWER DISSIPATION = 145 mW

DYNAMIC SWITCHING ENERGY = 0.48 pJ/GATE

PROPAGATION DELAY = 110 ps/GATE

Fig. 4.2-7 3 stage D flip-flip divider operation at 1.9 GHz clock.

A SEM photograph of a multiplexer chip is shown in Fig. 4.2-8. A corresponding schematic is shown in Fig. 4.2-9. The circuit includes a synchronous counter which may be used to generate sequential addresses to the address select portion of the circuit. Two clock enable inputs are provided, so that the clock input to the synchronous counter may be gated on or off. Preset and clear inputs to the counter are provided, so that any address can be set up without having to sequence through undesired addresses. One multiplexed input is provided for each of the eight addresses generated by the counter. A synchronous output decodes address 000. This output is useful as a reference signal when sequential addresses are generated, and also as an indicator that the counter has been cleared when preset and clear are used for address setup. An additional input is provided for on or off gating of this synchronous output. This input will be useful when the multiplexer is tested in conjunction with a demultiplexer. The multiplexed output is also fed into the data input of a D type latch. This latch may be clocked either from the clock provided to the counter through appropriate delays, or from a separate input. A separate input is provided for gating the internal clock to the latch. Q and $\overline{Q}$ outputs of this latch are provided. The latch is used to obtain output data free of unwanted glitches which could occur due to the finite (4 τ_D) setting time of the synchronous counter. The maximum clock rate of the circuit is limited by the synchronous counter and was determined to be f_{max} = 1/5.2 τ_D by logic simulation.[1]

Figure 4.2-10 shows the relationship between the output signal and the input clock signal at a low clock frequency (10 MHz) as previously reported[2]. The top photograph on Figure 4.2-10 shows the output of the multiplexer with one input selected, for one complete cycle of the counter. The bottom photograph in Figure 4.2-10 shows the output with two inputs (3 and 5) selected. An input is selected by biasing it to V_{DD} through a 4.7 KΩ resistor. These output bit patterns repeat every 8 clock cycles.

Figure 4.2-11 shows the multiplexer output with one out of eight inputs selected, while the multiplexer was operating at a 1.1 GHz clock frequency

SC79-3584

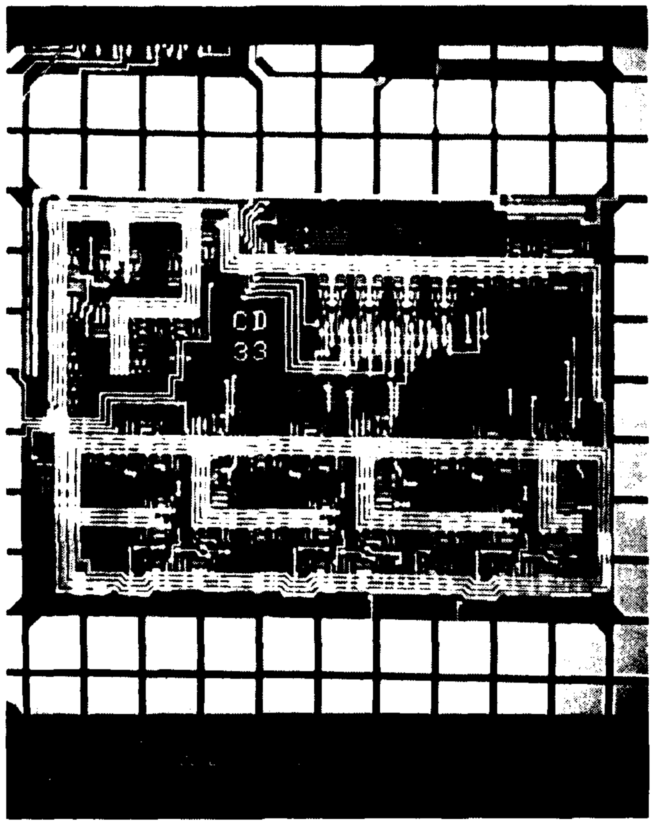


Fig. 4.2-8 SEM photograph of an 8 input data multiplexer chip containing 64 gates.

SC79-3590

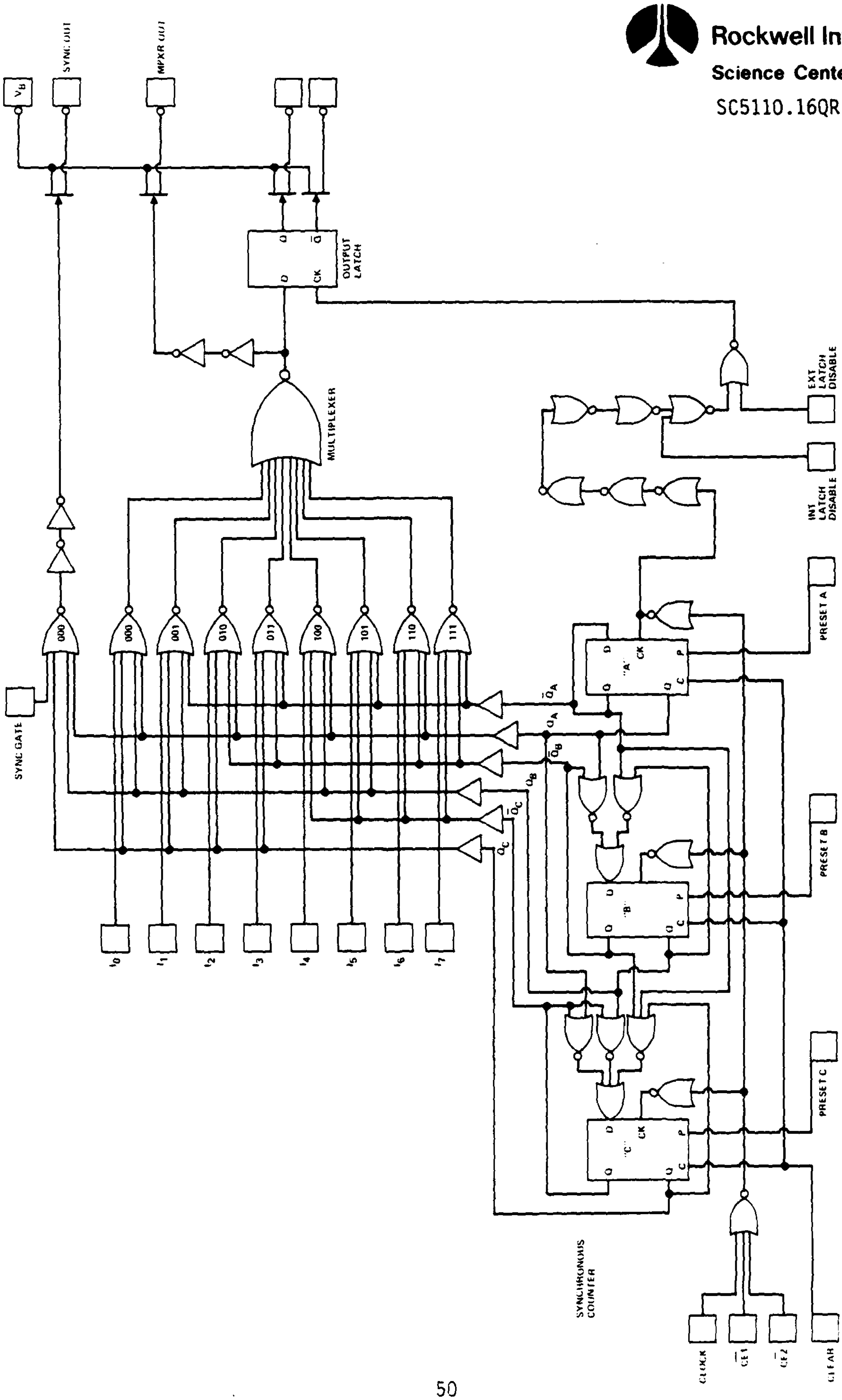


Fig. 4.2-9 Schematic of multiplexer circuit. (from ARPA Sixth Quarterly Report[2])

SC79-3810

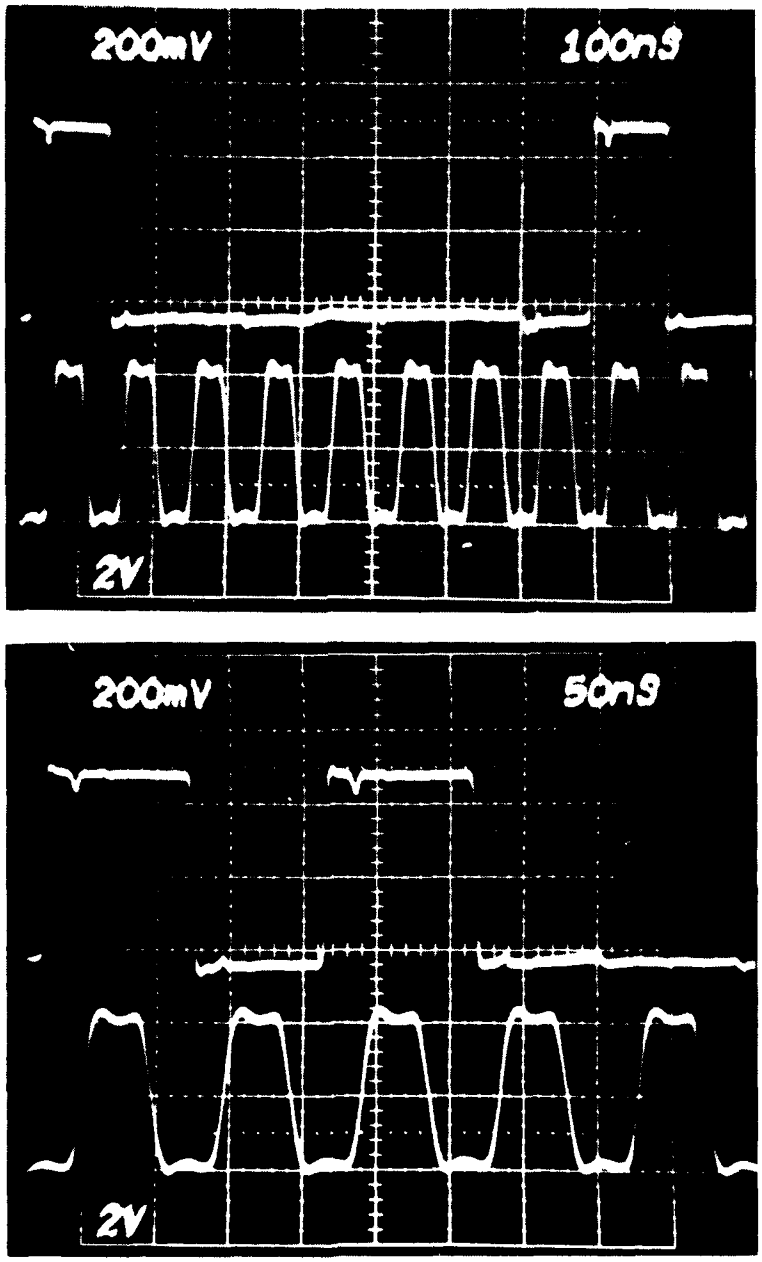


Fig. 4.2-10 Oscillograms showing multiplexer outputs (upper traces) and clock inputs (lower traces), (a) for one input "high", (b) for two inputs "high". (From Sixth Quarterly Report.[2])

SC79-4707

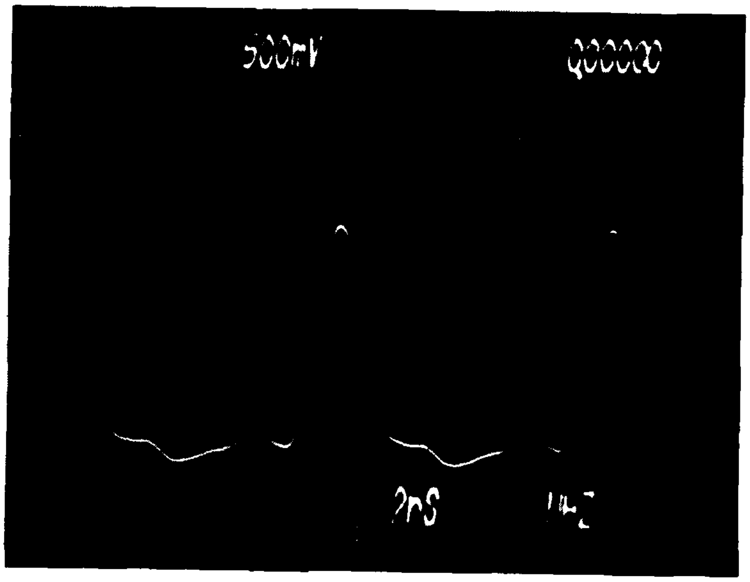


Fig. 4.2-11 Oscillogram showing multiplexer output at 1.125 GHz clock input.

The maximum clock frequency at which this circuit would function was 1.125 GHz. The output measurement was taken on a sampling oscilloscope; however the bandwidth was limited by the 0.9 GHz Tektronix FET probe used to monitor the output voltage. Figure 4.2-12 shows the multiplexer output with two out of eight inputs selected, operating at a 0.7 GHz clock frequency. This output waveform repeated every eight clock cycles as expected. As many combinations of inputs as could be accessed with the limited number of probes available were tested and were found to function as expected.

These recent results represent a significant improvement in speed over previously reported data[2] in which operation was limited to clock frequencies of 225 MHz or less. The 1.1 GHz clock performance is in good agreement with theoretical performance limits of the synchronous counter and dynamic performance of SDFL NOR gates. The best speed-power product achieved was 0.85 pJ/10 μm NOR gate at an equivalent propagation delay of 170 ps.

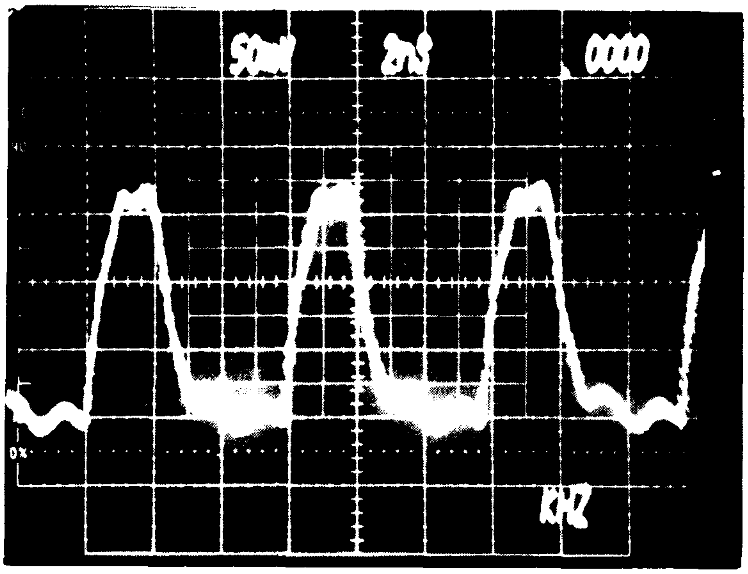
The power dissipation of the multiplexer circuits ranged from 75 mW (with a pinch-off voltage of -0.5 V)[2] to 430 mW with a pinch-off voltage of -1.454 V. The power dissipations for this circuit are higher than expected, and this is attributed to voltage drops along the supply bus lines requiring higher supply voltages in order to make the circuit functional. This could be alleviated by improving the layout such that the lengths of the supply lines are shortened and/or by widening the supply lines.

The input to 8-output data demultiplexer is located in subchips CD31 and CD53 of mask set AR2. This circuit connects the data input to one of the eight outputs on each clock cycle holding this connection for one full clock cycle. This type of circuit is useful for high speed serial to parallel conversion which could be applied to a gigabit data transmission link.

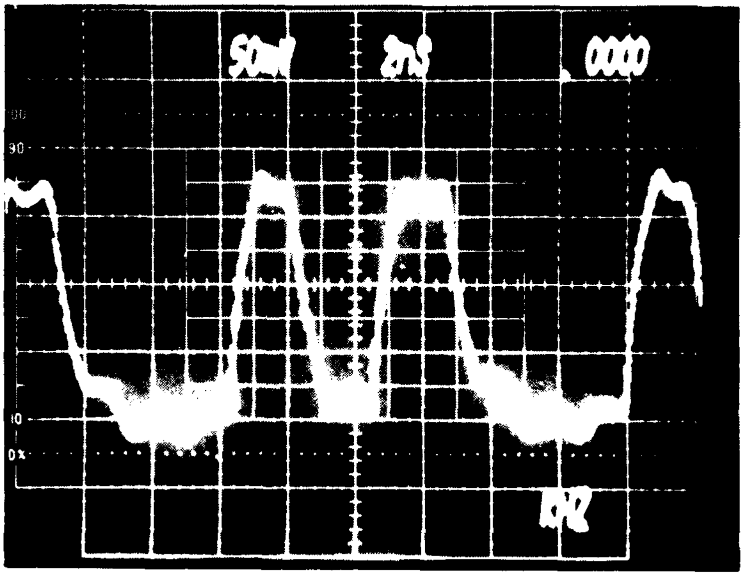
A schematic of the demultiplexer circuit is shown in Fig. 4.2-13. A SEM photograph of an actual circuit is shown in Fig. 4.2-14. The synchronous counter portion of the circuit is identical to that of the multiplexer circuit discussed previously. The input signal, which is gated to all eight outputs, can be strobed by the input clock, when the gating override input is not

MULTIPLEXER OUTPUT
CLOCK FREQ. = 700 MHz

SC79-4391



INPUTS 3 AND 7



INPUTS 3 AND 6

Fig. 4.2-12 Multiplexer output with two data inputs selected.

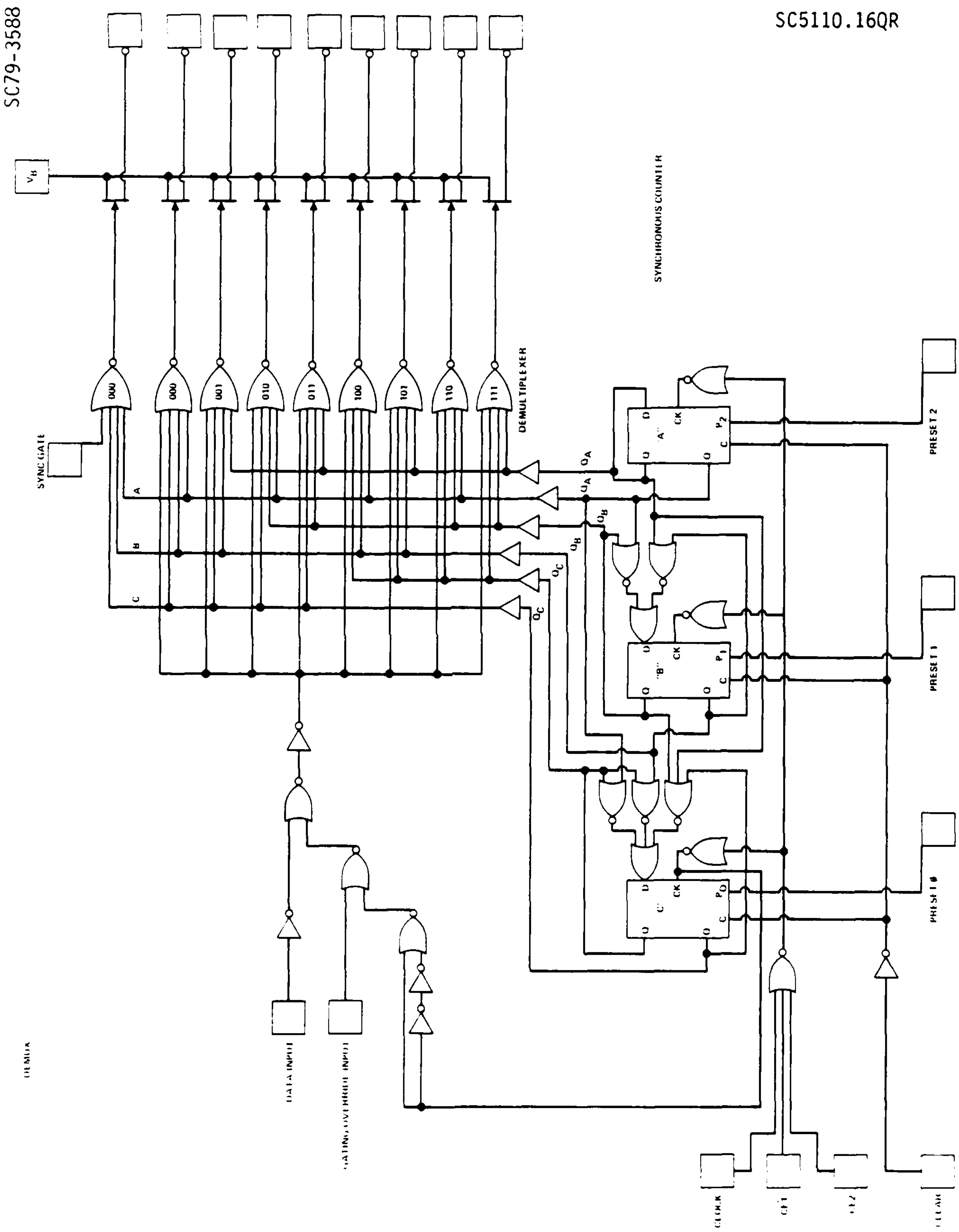


Fig. 4.2-13 Schematic diagram of the 1:8 data demultiplexer.

SC79-4377

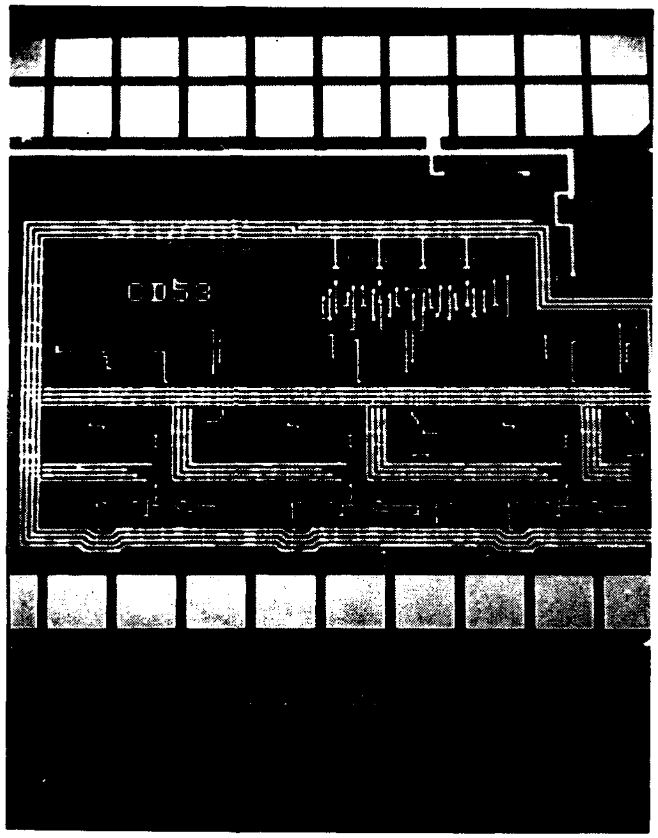


Fig. 4.2-14 SEM photograph of the 1:8 data demultiplexer.

exercised. When the counter's outputs decode the address of one of the eight NOR gates, any signal on the input will then appear on the output whose address was decoded.

Operation of this demultiplexer was achieved during the past reporting period at clock frequencies as high as 1.0 GHz. This performance, similar to that of the multiplexer, is in good agreement with theoretical expectations. The circuit was evaluated by biasing the data input at V_{DD} so that a repetitive 1/8 duty cycle waveform could be observed on any output. Figure 4.2-15 shows the output of the demultiplexer at clock frequencies of 254 MHz and 1.025 GHz. The lower frequency data also shows the clock signal as a reference to demonstrate that one output out of eight was selected every eight clock cycles. Bandwidth of this data was again limited by the probes.

Figure 4.2-16 shows the result of another measurement in which the 250 MHz generator was connected to the data input. Here, it can be seen that this burst of pulses is properly selected or routed to the appropriate output for one out of every eight clock cycles. The lower photograph provides an expanded view of one such burst with part of the clock also visible.

The power dissipation for this circuit ranged from 315 to 400 mW with a pinchoff of -1.45V. Again, this power dissipation is higher than expected for the same reasons attributed to the high power dissipation for the multiplexer circuit. The speed power product is 1.06 pJ/gate. This circuit was operated with an input clock as high as 1.06 GHz. The corresponding calculated propagation delay is 181 psec/gate.

In conclusion, the results obtained so far concur with those expected from the results of the logic simulation programs and the ring oscillator tests. The multiplexer and demultiplexer circuits, both with >60 gates each, represent the largest (in number of gates) GaAs ICs successfully evaluated at any speed. Maximum operating frequencies of approximately 1.1 GHz were achieved for both circuits, while ripple counters (25 gates) functioned as high as 1.9 GHz. Equivalent propagation delays as low as 110 ps/gate in the D flip-flop were observed. Since the DFF chain contains gates with fanouts of

SC79-4708

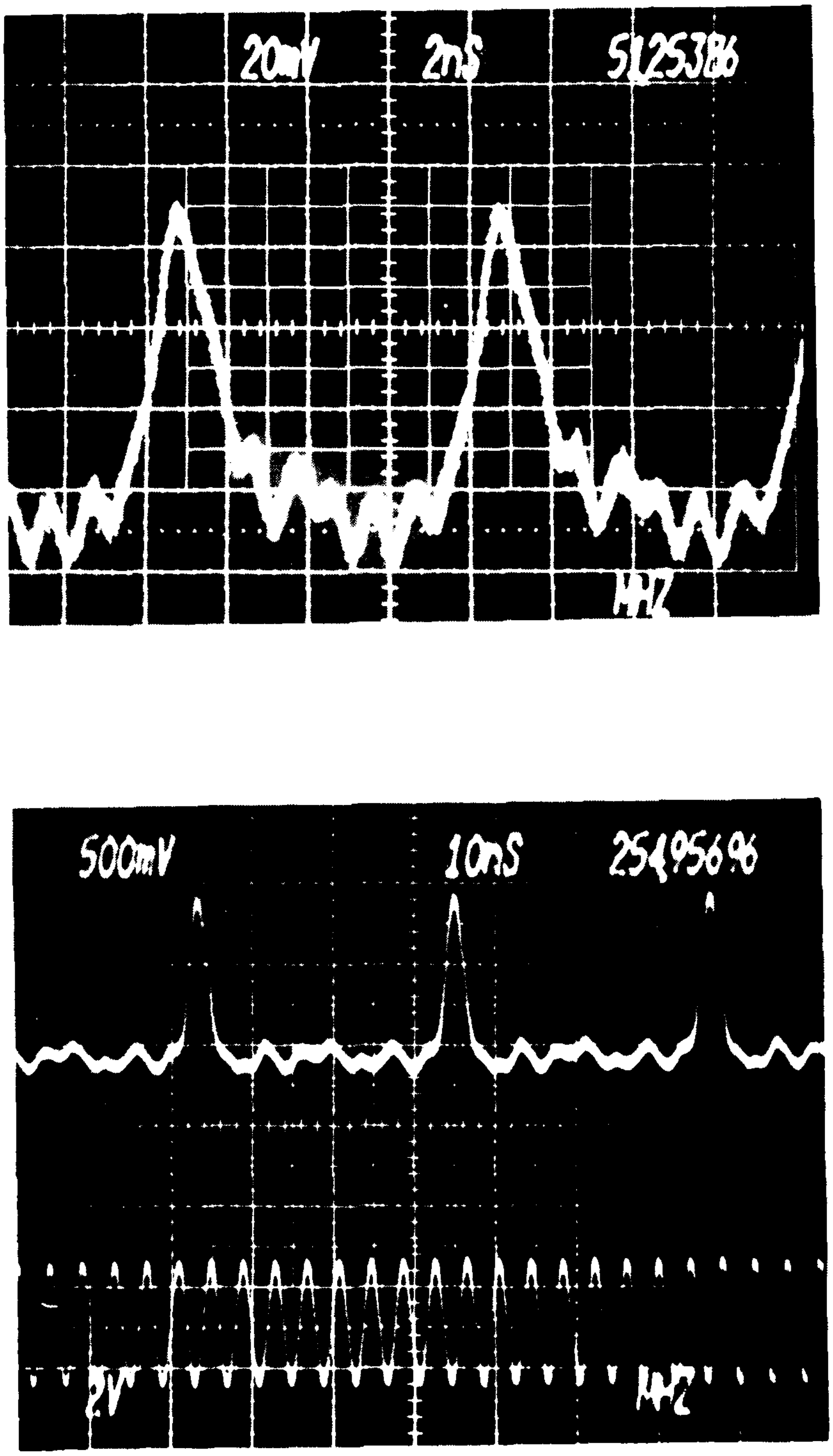


Fig. 4.2-15 Demultiplexer output at 254 MHz (bottom) and 1025 MHz (top) clock frequencies.

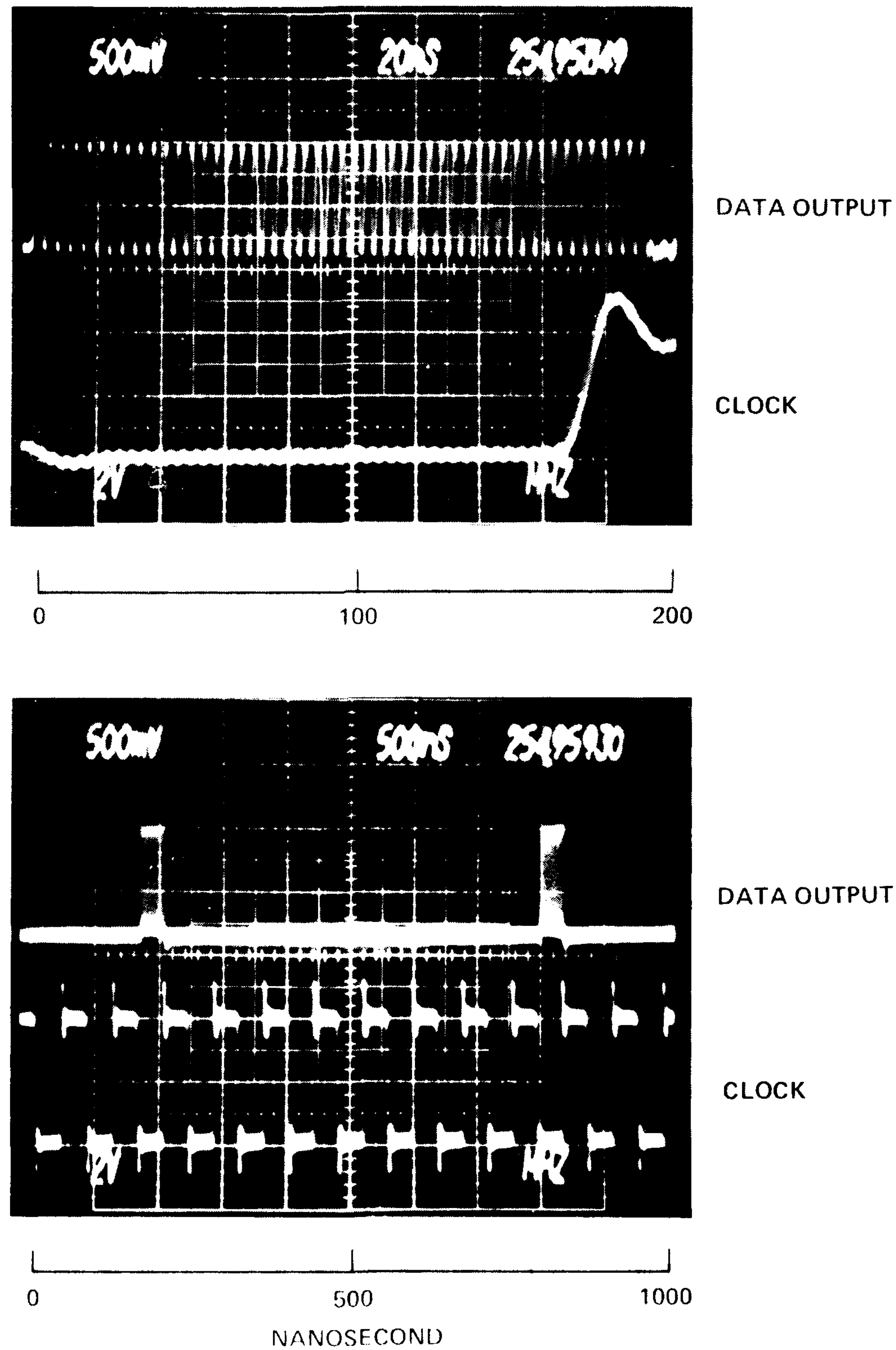


Fig. 4.2-16 Demultiplexer output and clock input with 250 MHz data source. The lower photograph presents an expanded view of the output burst.

2 to 4 and is a sequential logic circuit, this high speed performance clearly shows that the SDFL circuit approach is not limited to low speeds or low fan-outs and is competitive in speed to buffered FET logic designs while requiring significantly less power.

5.0 CIRCUIT DESIGN

In the first phase of this program, evaluation and development of the planar, SDFL process technology was centered around the use of mask sets AR1 and AR2. The first mask set, AR1, was carefully designed to allow for experimental variation of several key device and process parameters on a single wafer. Detailed evaluation of the circuits fabricated using this mask set led to refinements in design rules. A maximum circuit complexity of 10 gates was imposed on AR1 in order to focus most of the effort onto key process and device design considerations. Encouraging yields of circuits at the 10 gate level of complexity suggested that the next mask set should include some attempts at MSI circuits of 50 to 75 gate complexity. Therefore, circuits of the MSI level gate complexity were designed and implemented on the second mask set AR2. Circuit evaluation on the AR2 mask set has been carried out. Proper operation of the ripple counter, 8 input data multiplexer and corresponding demultiplexer at a clock rate in excess of 1.1 GHz has been achieved. Good yield has also been found on the long chain of NOR gates (98 gates). These results strongly indicate that an even higher gate complexity circuit should be implemented on the third mask set.

5.1 AR3 Demonstration Circuits (Electronics Research Center)

The design, digitization and fabrication of the third mask set AR3 has been completed. It contains circuits with increased complexity over AR2, including a latched demultiplexer with gate complexity of 103. The basic 9-chip organization, lot size and pad configuration of earlier mask sets have been retained. Because many of the process monitoring and development test cells on AR1 and AR2 have already been evaluated, the process development (PD) chip included on the earlier mask sets has been redesigned and merged into the process monitor (PM) chip. The MSI demonstration circuits are located in a circuit development (CD) chip such as was introduced on AR2.

A schematic of the AR3 mask layout is shown in Fig. 5.1-1. The top portion of this figure shows how the mask is organized into nine chips, with a process monitor (PM) chip in the center surrounded by 8 circuit development (CD) chips. The dimensions indicated on the figure are final dimensions on the wafer. The mask is actually four times larger to accommodate the 4X reduction provided by the projection mask aligner (PMA). This mask will be stepped by the PMA in either 2 × 2 or 3 × 3 arrays.

The PM chip has been redesigned eliminating some test patterns that are no longer necessary, refining the design of others, adding some new test patterns, and incorporating test patterns that were previously located on the PD chip no longer in use. A photograph of PM is shown in Fig. 5.1-2. The PM chip contains three types of test patterns. The first type consists of tests for direct evaluation of fabrication steps, such as implantation profile test patterns for C-V measurements, ohmic contact resistance test patterns, metalization line resistance tests, over-crossing and interconnect integrity tests, sheet resistance and linewidth test patterns for each of the implanted layers, and electrical alignment test patterns for some of the critical alignment steps. National Bureau of Standard test patterns have been used for the sheet resistance and linewidth measurements[8,9] and for the electrical alignment measurements.[10] The second type of test pattern relates to device design. These test patterns have been and are being used for design rule development. For example, an experiment on the effects of purposely introduced misalignment on FET characteristics is being conducted using test patterns in PM. FET and diode arrays containing 81 and 100 devices, respectively, have been designed for monitoring short range variation of device characteristics. The arrays will be tested with the automatic measurement system. Finally, a third group of test patterns in the PM test area include two long chains of gates (84 and 98 gates), a D flip-flop with all its internal nodes connected to pads for low frequency monitoring of its waveforms, and ring oscillators used for quick evaluation of speed and power dissipation performance.

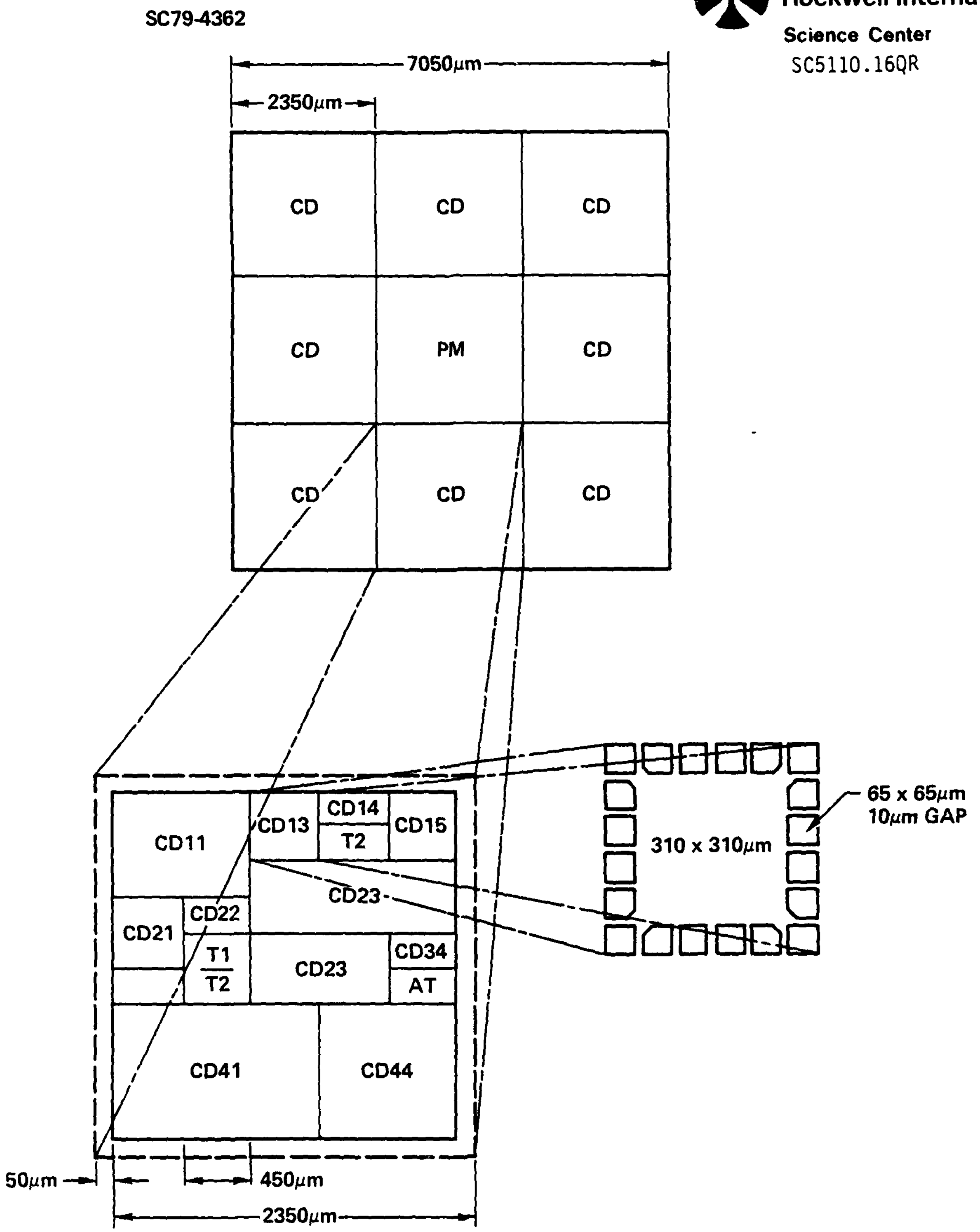
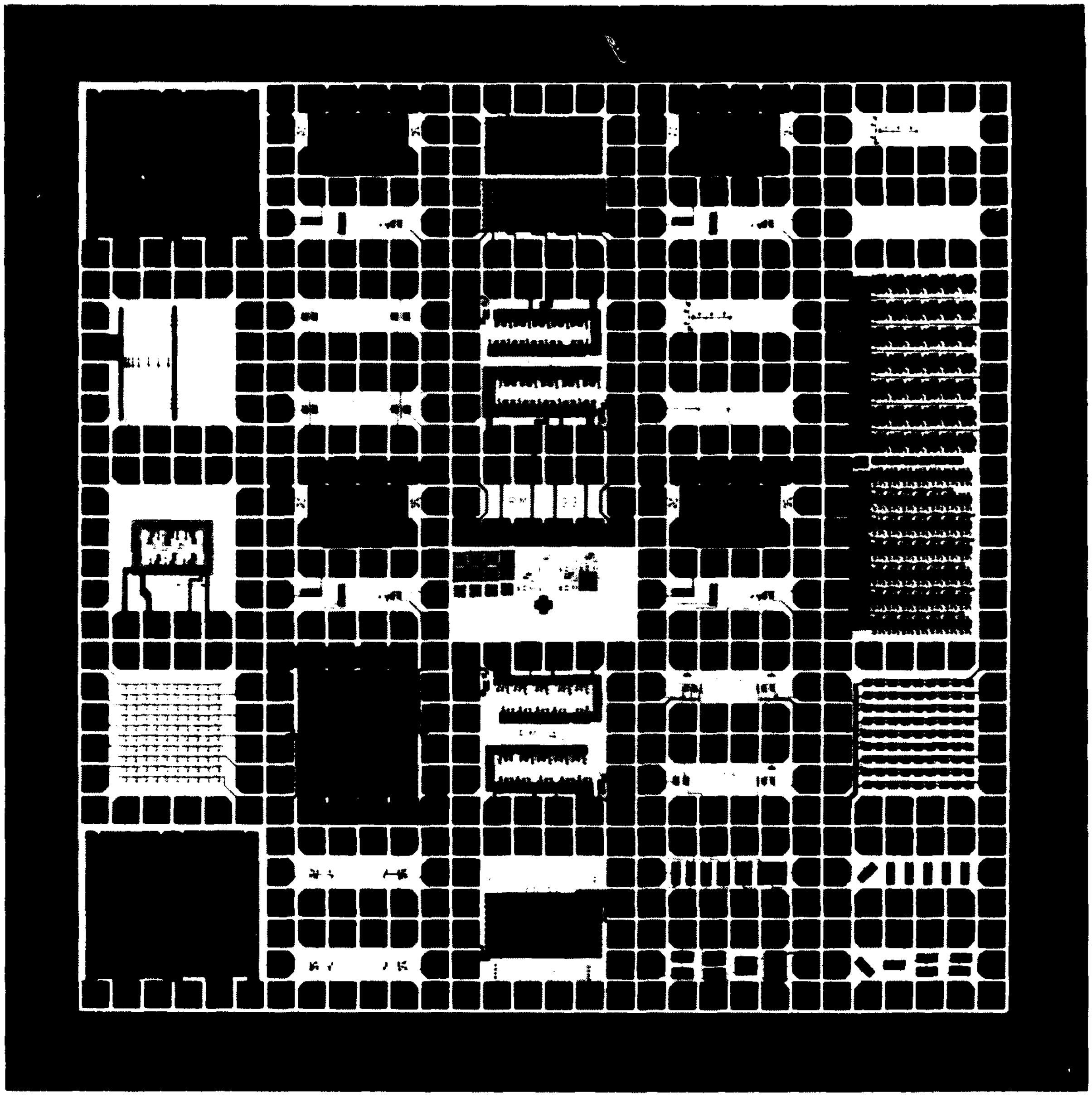


Fig. 5.1-1 AR-3 mask layout schematic.

SC79-4709



ROCKWELL SCIENCE CENTER AR3-PM - ■

Fig. 5.1-2 Photograph of the process monitor (PM) chip for mask set AR-3. The overall dimensions are 2.25 x 2.25mm.

The test patterns, labeled T1/T2, are similar to the ones used in mask sets AR1 and AR2, but they have also been redesigned. They consist of a small, 450 μm × 450 μm, test cell containing the most essential process monitoring test patterns and the most critical devices. This cell is also at two locations on the CD chip. This assures a dense and uniform distribution of T1/T2 cells over the wafer, so that process uniformity can be assessed using an automatic measurement system. A detailed view of T1/T2 is presented in Fig. 5.1-3. T1 contains C-V and sheet resistance test patterns for the critical implanted layers, namely the n^- layer for the FET channel and the n^+ layer for the Schottky diodes. In addition, T1 contains an ohmic contact test pattern and a substrate isolation test pattern. The major design change in T1 was the incorporation of the C-V test patterns made possible by the considerable space savings achieved using small sized NBS sheet resistance test patterns. T2 contains FETs and a logic gate with all its nodes connected to pads. This gate is used to monitor the characteristics of its individual components, and also to test its overall operation (at low frequency). T2 has undergone only minor revisions with respect to the previous design.

The circuit development chip will now be discussed. A subdivision of this chip is shown in the lower half of Fig. 5.1-1. This chip is composed of 15 lots consisting of 1/2 × 1, 1-1/2 × 2, 1 × 2, 1 × 3, 2 × 2 and 2 × 3 multiples of the basic single lot shown at the right. An index of the circuits contained on CD is shown in Fig. 5.1-4. Fig. 5.1-5 shows a photograph of the CD chip of AR3. The ring oscillator and cell T1/T2 are identical to those on PM. The rest of the circuits are counters, multipliers, a shift register, a multiplexer and a demultiplexer, and component parts of the above. The circuits approach or exceed MSI complexity.

A 3-bit by 3-bit parallel multiplier with a total gate count of 75 is located on chip CD 11. The operations required to multiply two 3-bit binary numbers ($B_2B_1B_0 \times A_2A_1A_0 = P_5P_4P_3P_2P_1P_0$) are illustrated in Fig. 5.1-6(a). The addition process in the multiplication is accomplished by properly combining full adders and half adders as shown in the block diagram of

SC79-4710

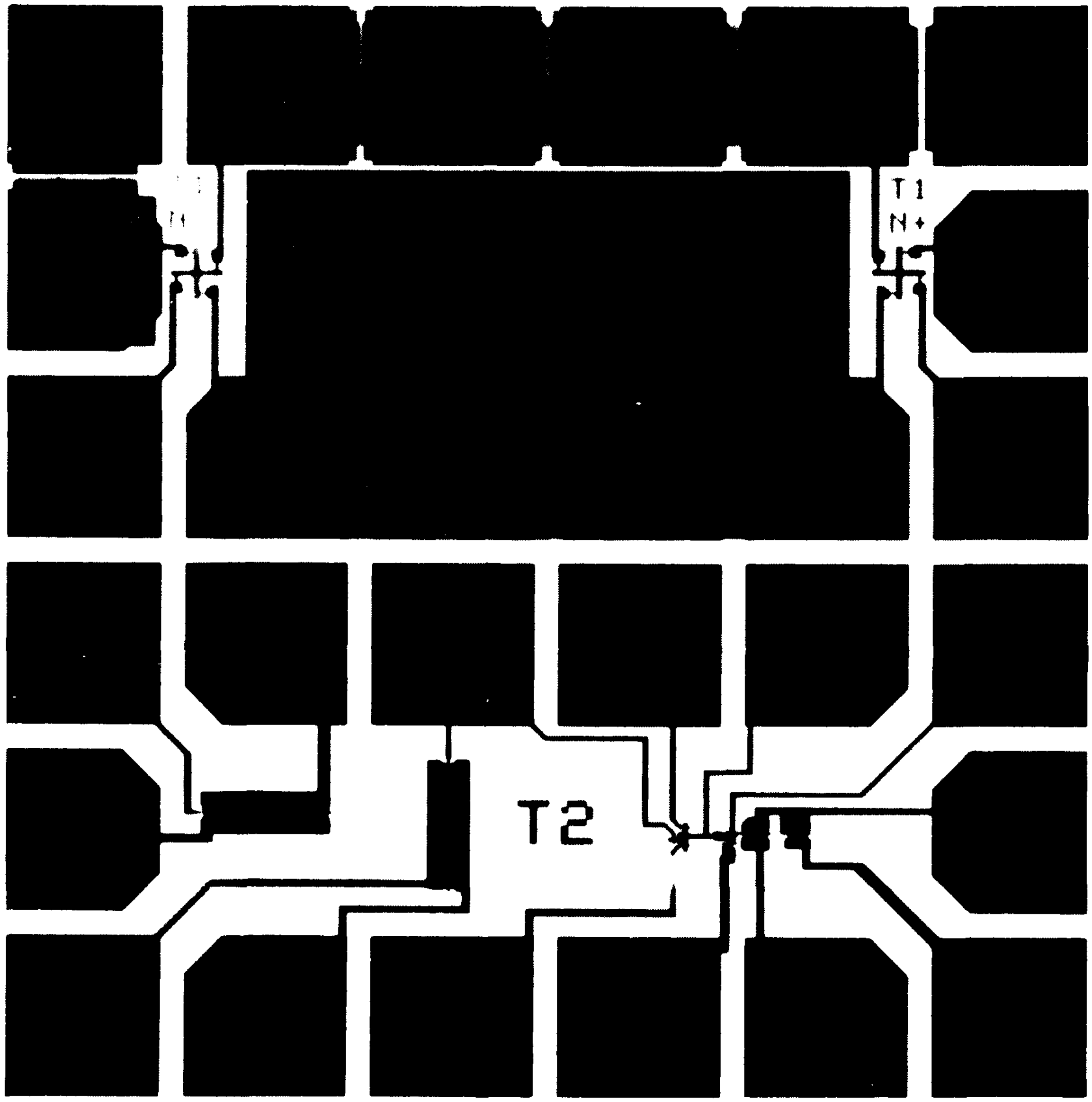


Fig. 5.1-3 Photograph of the T1/T2 test cells on mask set AR-3. Contact pad dimensions are 65 x 65μm.

MASK SET AR-3

CD CHIP

SC79-4056

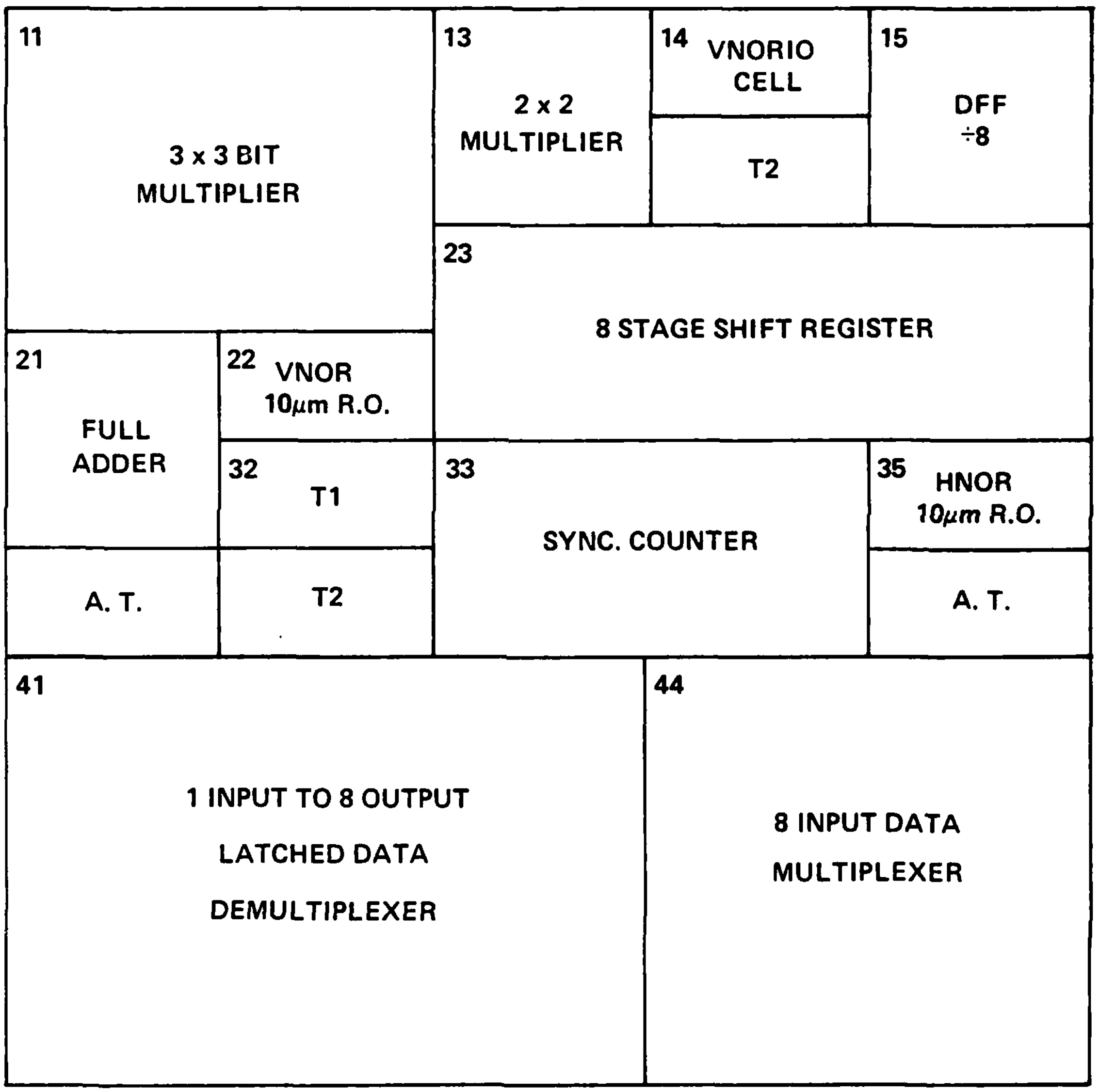
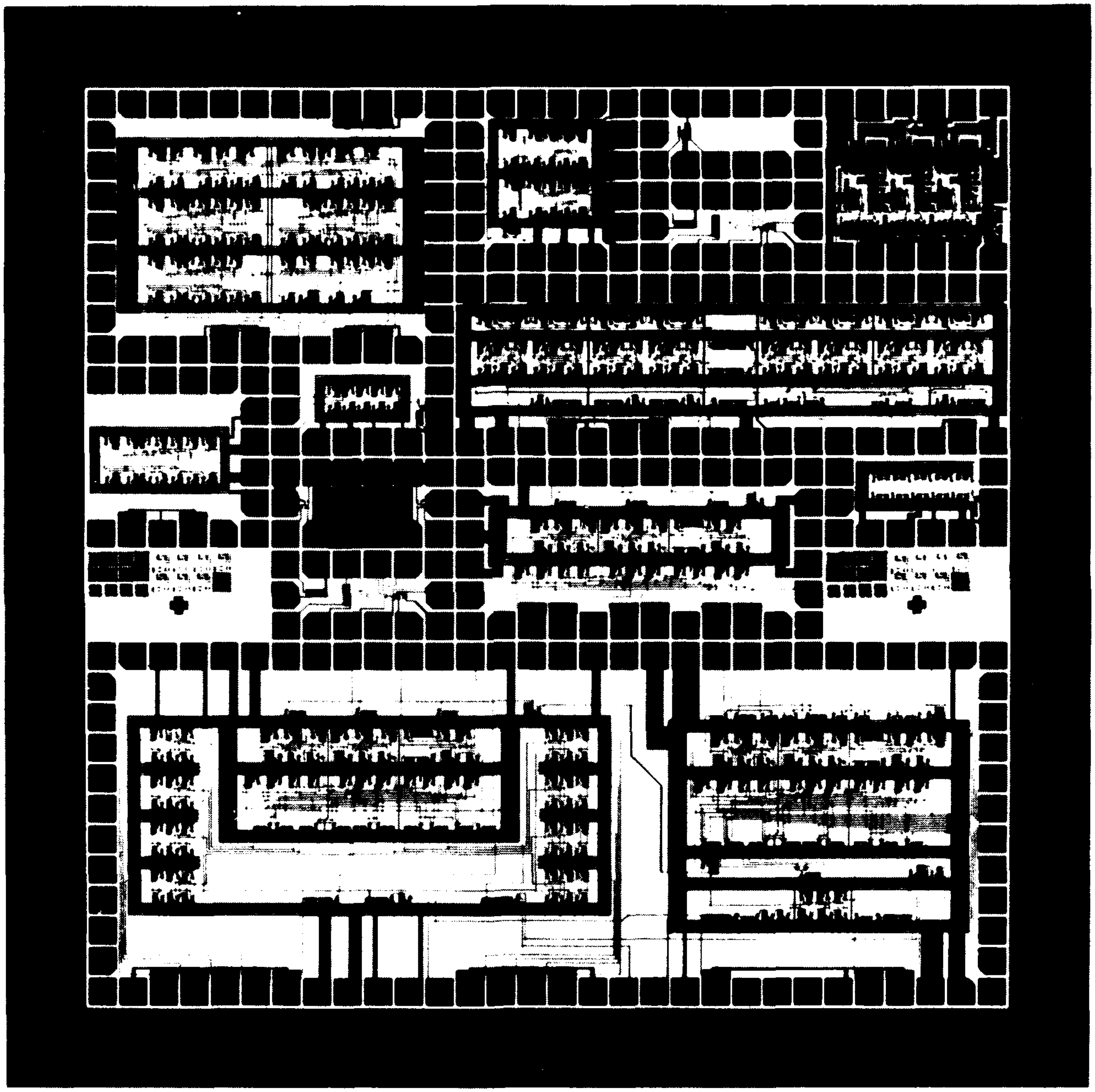


Fig. 5.1-4 Lot assignment map for circuit development chip (CD) on mask set AR-3.



ROCKWELL SCIENCE CENTER AR3-CD -

Fig. 5.1-5 Photograph of the circuit development (CD) chip on mask set AR-3. The overall dimensions are 2.25 x 2.25mm.

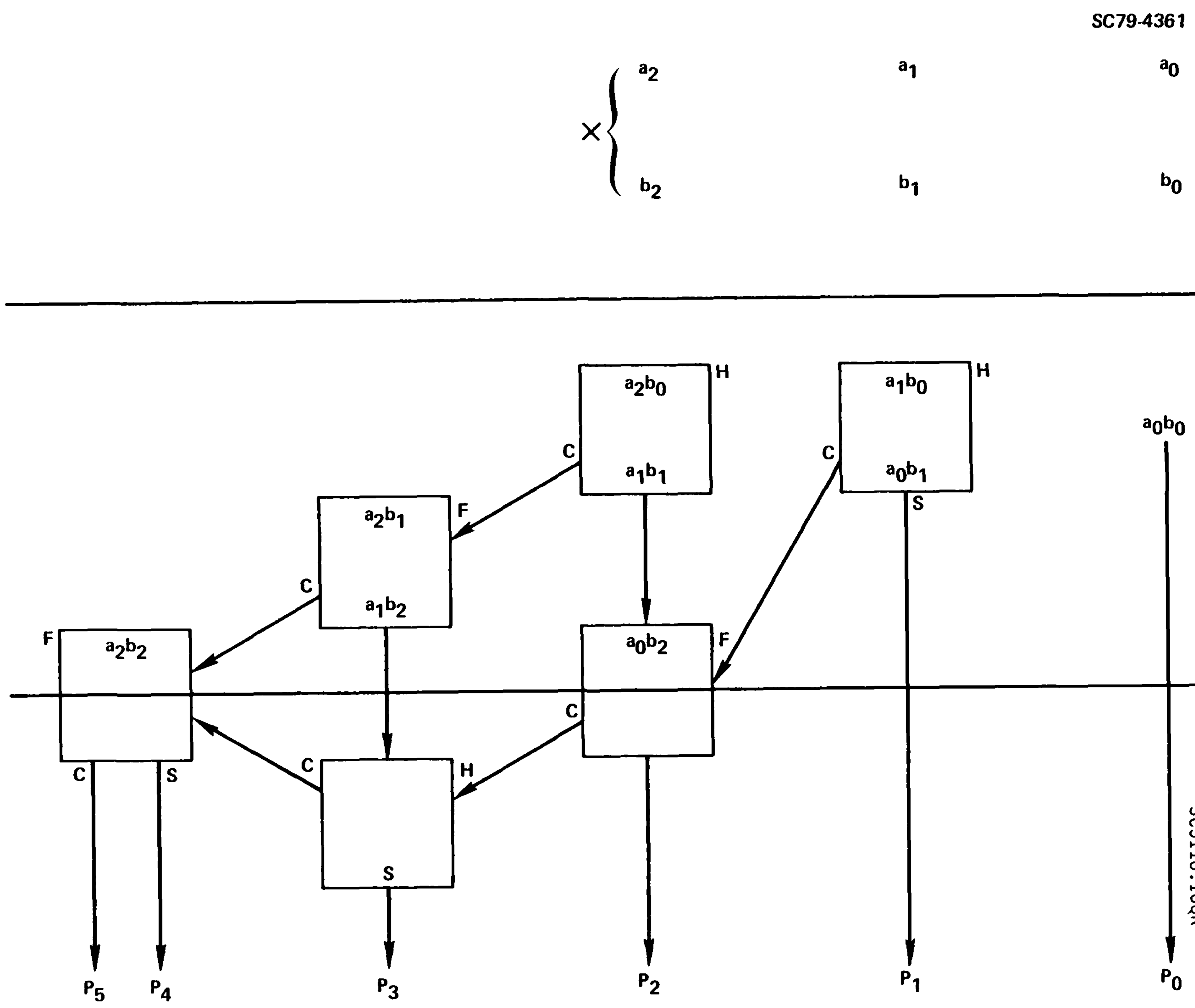


Fig. 5.1-6(a) Procedure for multiplying two 3 bit binary numbers.

SC79-4059

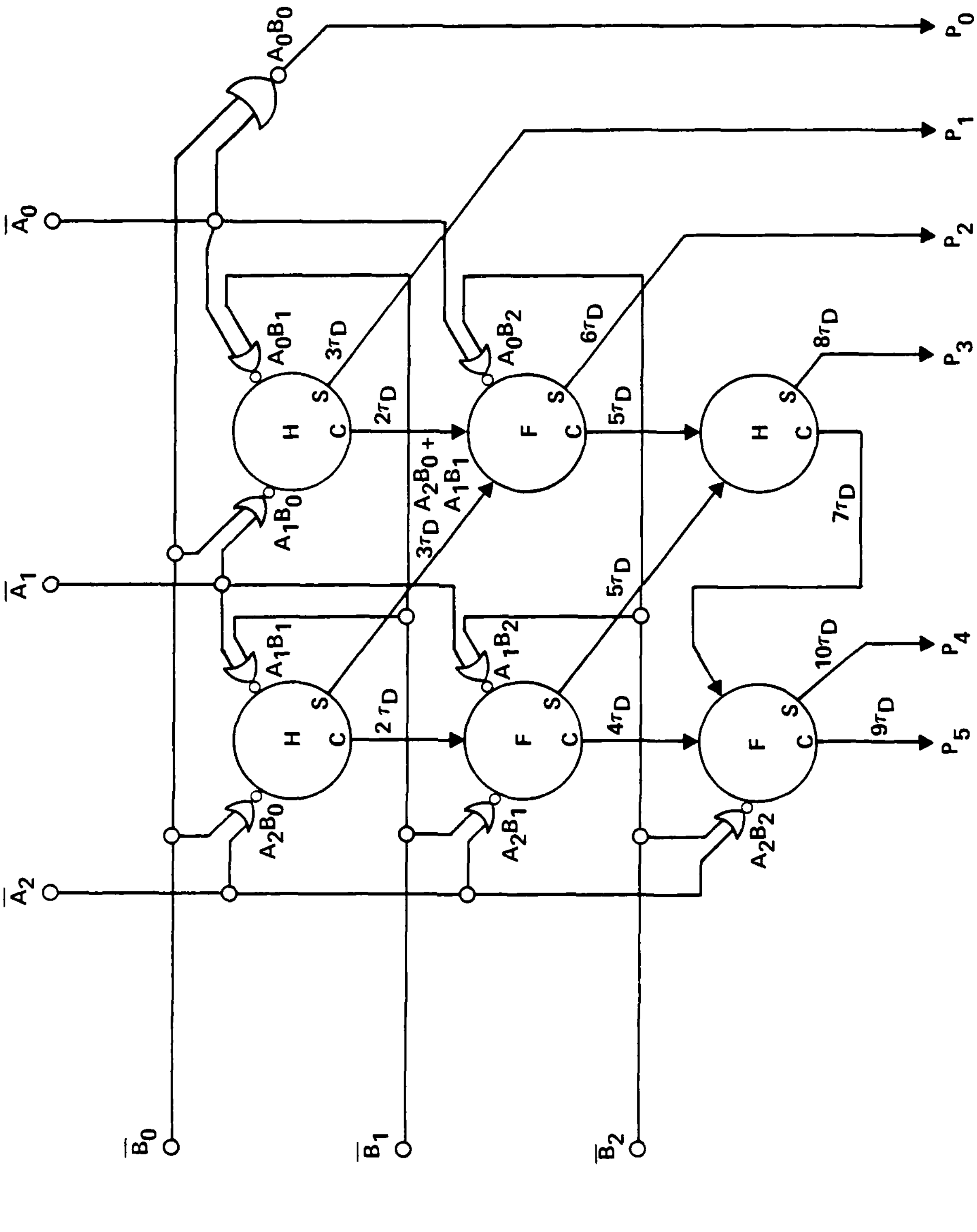


Fig. 5.1-6(b) Block diagram of a 3x3 parallel multiplier.

Fig. 5.1-6(b). Three half adders and three full adders are used. Schematic diagrams of the SDFL NOR gate implemented half adder and full adder are given in Figs. 5.1-7(a) and (b), respectively. A photograph of the 3 × 3 multiplier is shown in Fig. 5.1-8.

In order to ease the evaluation of the propagation delay of a multiplication process (estimated less than 1 nsec), an optional NOR control gate and a feedback loop from P_5 (the most significant bit of the product) to A_0 (the least significant bit of the multiplicant) has been added to build a special ring oscillator-like multiplier (see Fig. 5.1-9). During the normal multiplication process, a logic "1" voltage will be applied to the control NOR gate such that the data of P_5 cannot be fed to A_0 through the control gate (the feedback loop will be disengaged). By presetting the multiplier $B_2B_1B_0$ to 111, the multiplicant $A_2A_0A_0$ to 100 and applying a logic "0" voltage to the disabled control, the multiplier will operate in the ring oscillator mode. Initially, the P_5 will be set to logic "0" state because 111 × 100 = 011100. With the feedback loop enabled, the "0" state of P_5 will be inverted to "1", and set the A_0 input to logic "1" state. Upon this change, a new multiplication process will be carried out, and the P_5 will be set to logic "1" (111 × 101 = 100011). This new state of P_5 will then be inverted to "0" and fed through the control gate to reset the A_0 back to "0". Repetitively operating in this mode, the 3 × 3 multiplier will perform like a ring oscillator. A logic simulation computer program has been used to analyze the ring oscillator operation of the 3 × 3 multiplier. It is found that the oscillating frequency will be 1/14 τ_D (see Fig. 5.1-10).

Figure 5.1-11 presents a photograph of the 8-bit shift register (or pseudo-noise P/N generator) in Lot CD23 having a gate count of 92. Eight D-type flip-flops (DFF) have been used. A schematic diagram of the SDFL NOR gate implemented DFF with preset and clear inputs is shown in Fig. 5.1-12. The DFF is triggered by the trailing edge of the input clock pulse. The data input information (logic state of the D input) is transferred to the Q output on the trailing edge of the clock pulse. The logic state of the Q output will

SC79-4071

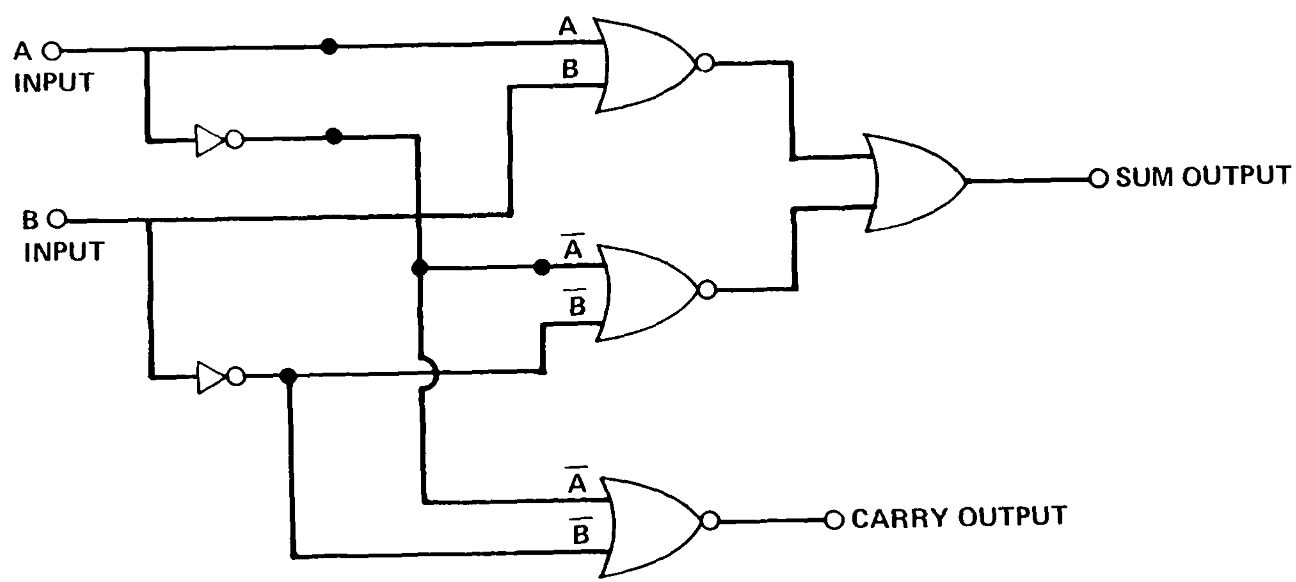


Fig. 5.1-7(a) Schematic diagram of a NOR implemented half adder.

SC78-2192

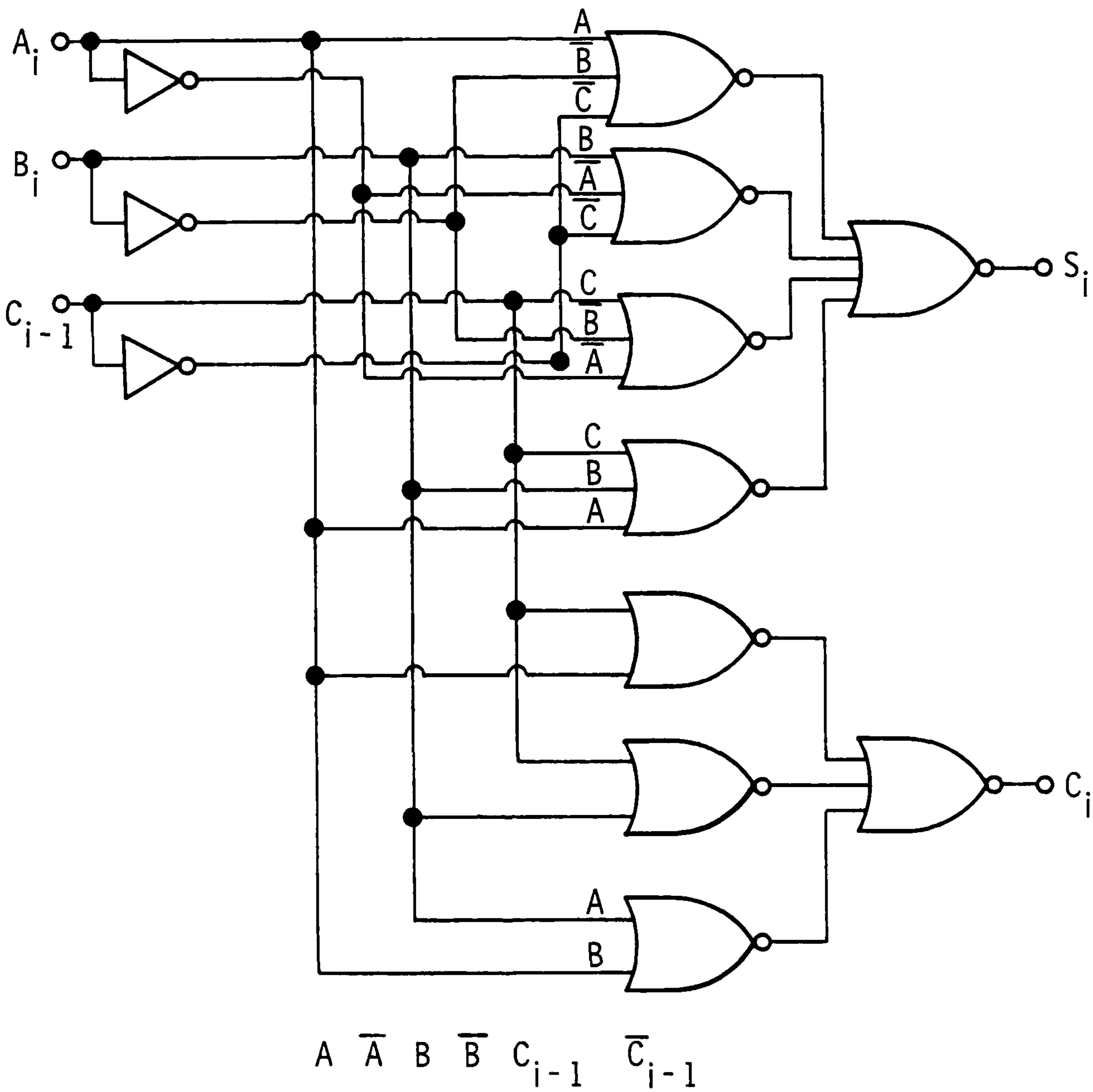


Fig. 5.1-7(b) SDFL NOR implemented full adder

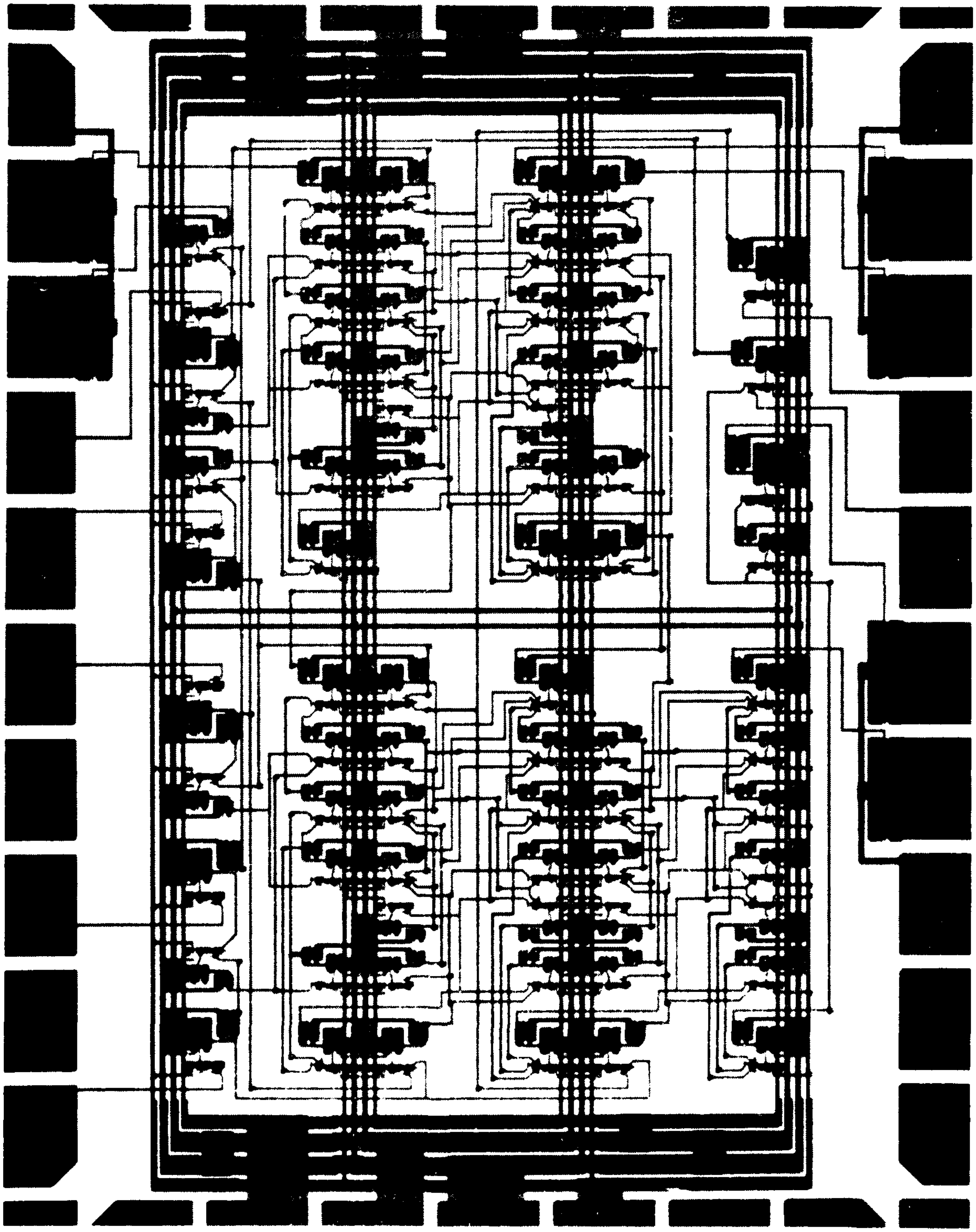


Fig. 5.1-8 Photograph of the mask overlay of the 3x3 multiplexer.

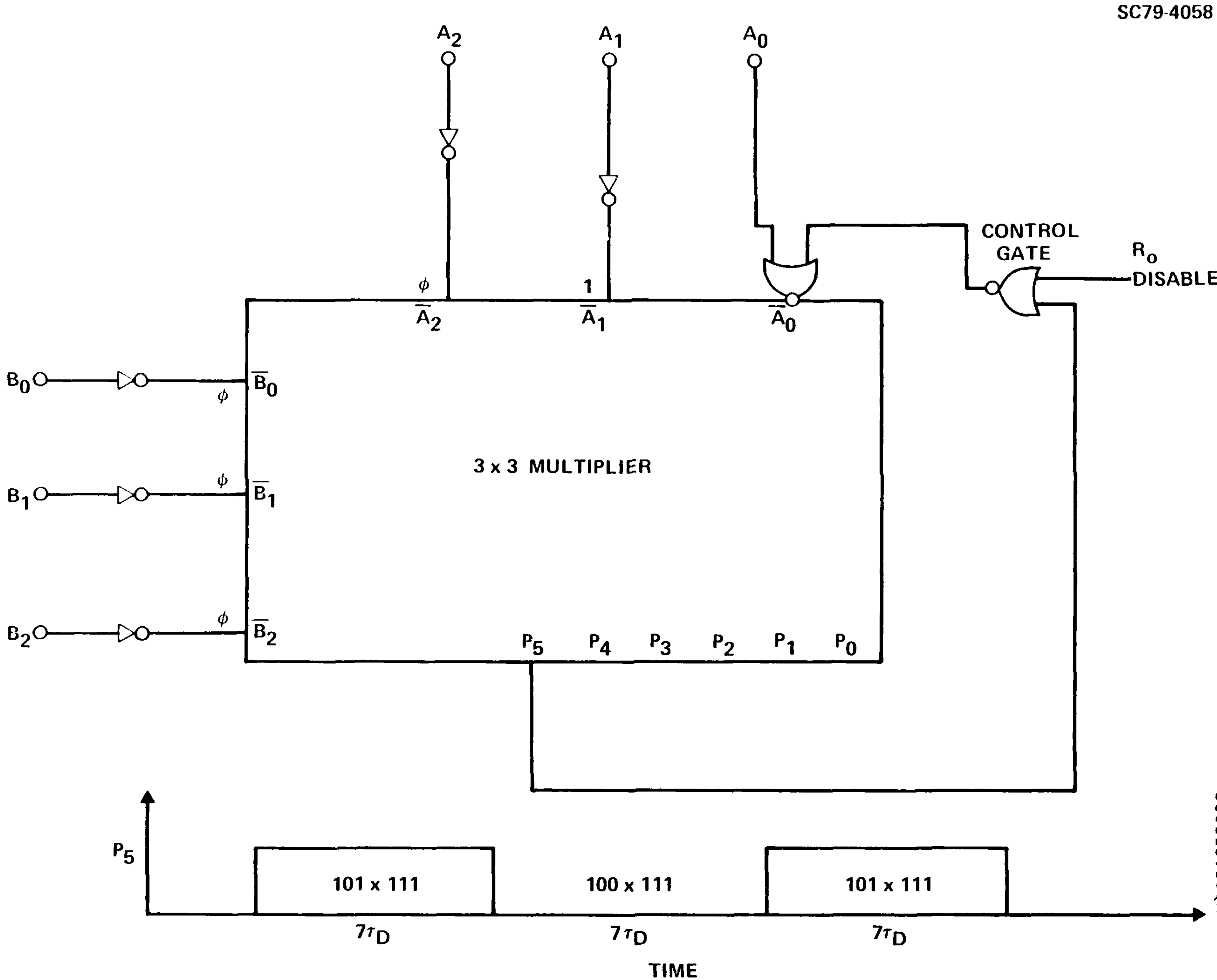


Fig. 5.1-9 Block diagram of a ring oscillator-like multiplexer and its output waveform.

SC79-4051

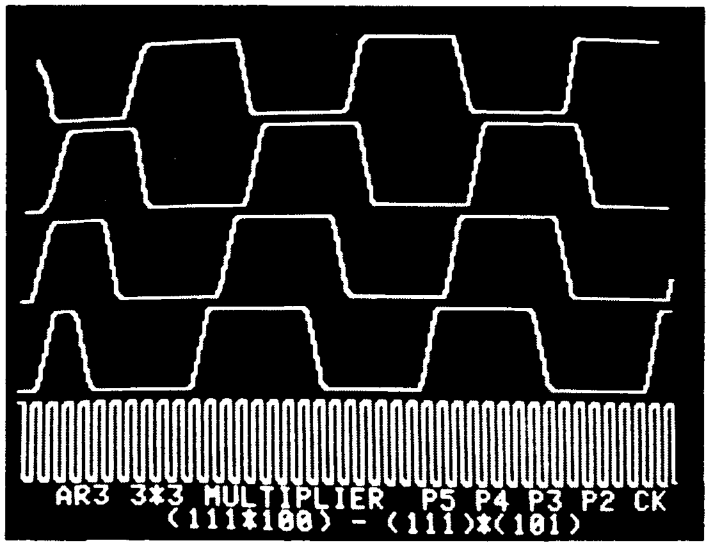
PRODUCT BIT 5 (LSB)

PRODUCT BIT 4

PRODUCT BIT 3

PRODUCT BIT 2

1 PROP DELAY REFERENCE



LOGIC SIMULATION OF 3 x 3 BIT PARALLEL MULTIPLIER WITH FEEDBACK

Fig. 5.1-10 Logic simulation of 3x3 bit parallel multiplier with feedback.

SC79-4713

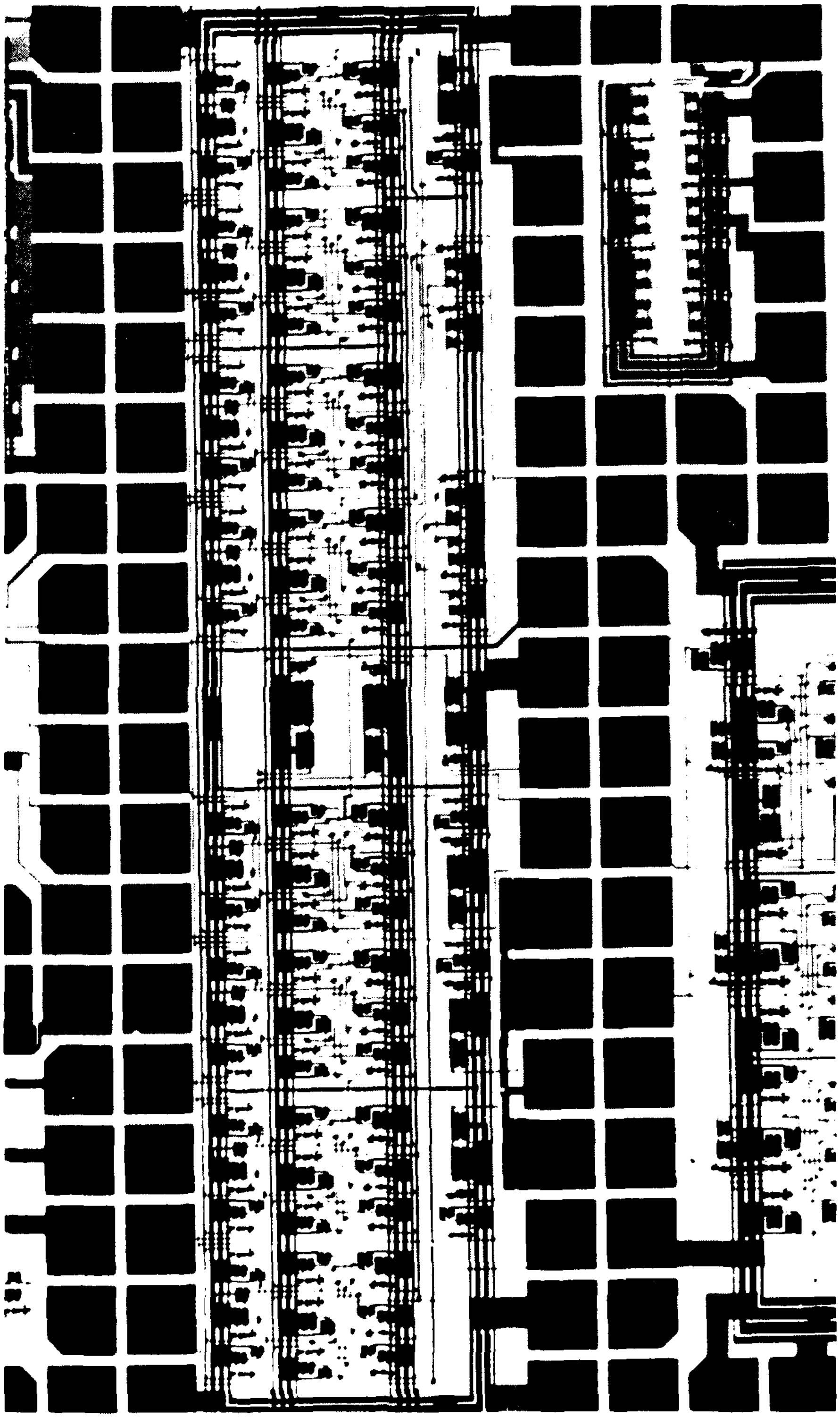


Fig. 5.1-11 Photograph of the 8-stage shift register color overlay.

SC79-4363

D-F.F. FLOP CELL IN SHIFT REGISTER OF AR3

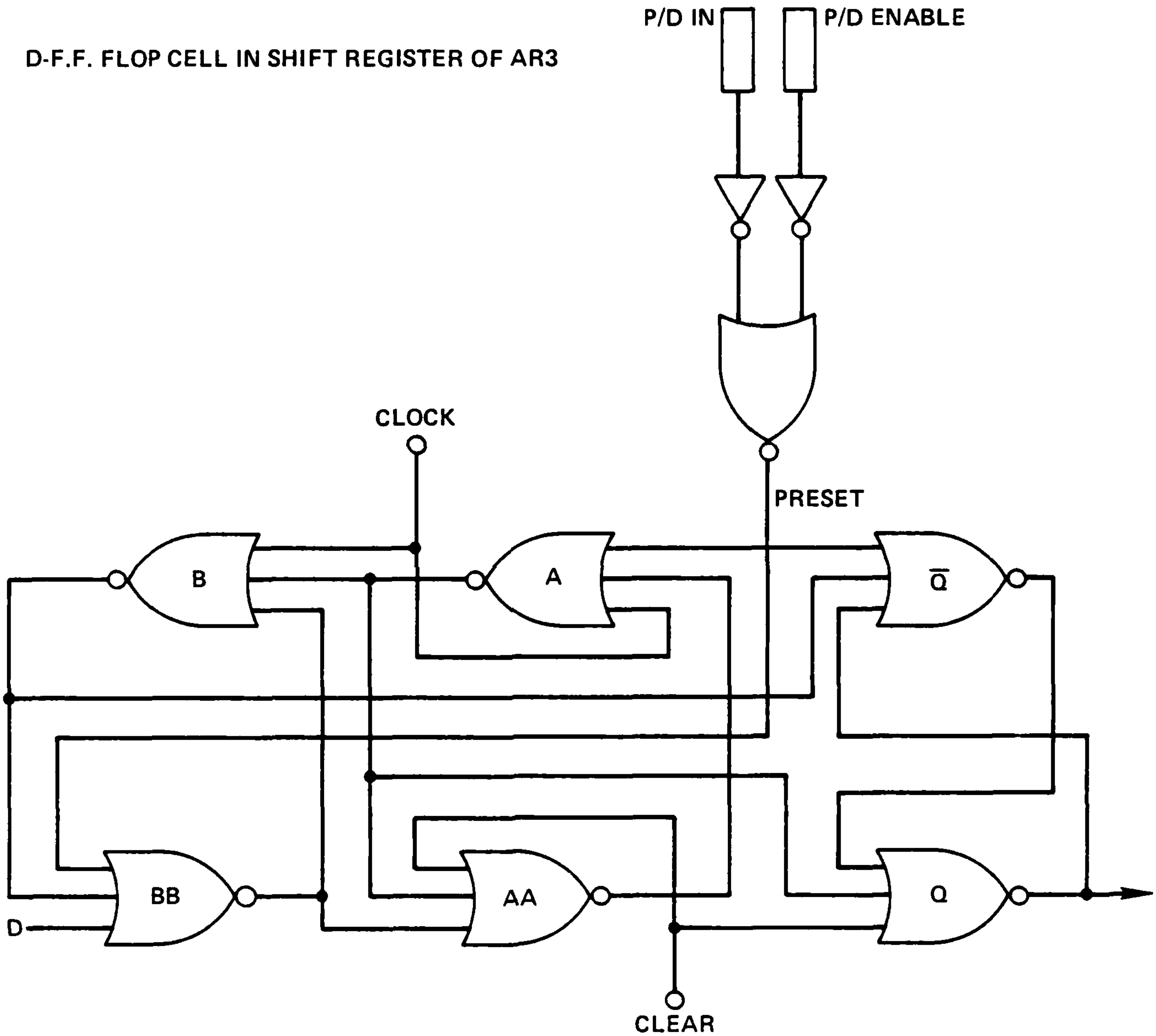


Fig.5.1-12 SDFL NOR implemented D flip-flip with preset, clear and preset enable.

remain unchanged until the next trailing edge of a clock pulse. Upon applying a logic "1" voltage to the clear input, the Q input will immediately set to logic "0" state. This condition can be applied independent of the state of clock input data input and present stored data. A logic "1" voltage applied to the preset input, while the parallel enable line has been held at logic "1" voltage, will set the Q output to the logic "1" state. With application of a logic "0" state of the parallel enable signal, the preset data input will not be able to transfer to the Q output of DFF.

In the shift register circuit, the Q output of the DFF is connected to the D input of the following stage. Therefore, at the trailing edge of the clock pulse, the information stored in the DFF is transferred to the next stage. Eight DFFs are serially cascaded to form an eight stage shift register. The clear inputs and parallel preset enable input of the eight stages are tied together, such that a logic "1" state applied to the common clear input will simultaneously set the Q output of all flip-flops to the logic "0" state and a logic "1" state applied to the common parallel preset enable line will be able to set each stage to the desired state simultaneously.

The Q output of the last stage DFF can be either directly connected to the first D input to form a circulating loop or exclusive-OR gated with the Q output of the 5th stage DFF, and then connected to the first stage D input to be operated in pseudo-noise generation mode. A recirculation enable line is designed to control the selection of the modes. A schematic diagram of the shift register circuit is given in Fig. 5.1-13.

Three clock input driver/inverter gates are used to square the input clock and increase the fan-out capability. The Q outputs of the 1st, 3rd, 4th and 8th stage are buffered and drive a bonding pad through a 65 μm source follower. From logic simulation results, it is expected that proper functioning of the shift register can be achieved up to a maximum frequency of $1/5.1\ \tau_D$. In the P/N generator mode, four different bit patterns can be obtained. The "A" mode, initialized by resetting flip-flop "A" to logic "1" and setting all others to "0", is the 217-bit pattern desired for the circuit. With different

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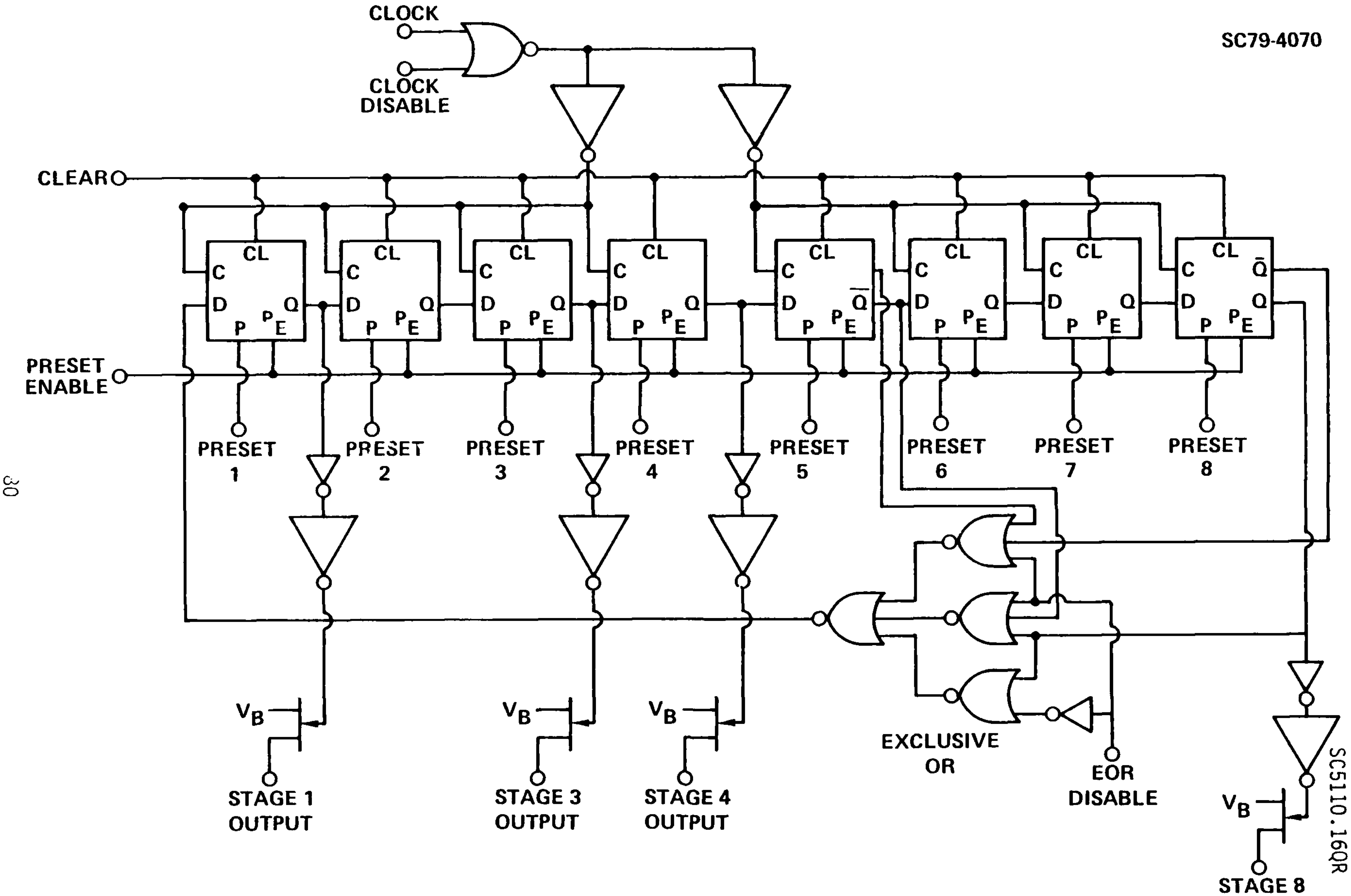

Fig. 5.1-13 Schematic diagram of the 8-stage shift register.

initialization, presetting A, B and D to "1" or resetting B, C, D and F to "1", the pattern generator can operate in a 31-bit or 7-bit code. The only remaining bit 00000000 will latch-up in its own state. The sum of this is $217 + 31 + 7 + 1 = 256 = 2^8$ possible states, as expected.

Lot DC-15 contains a binary ripple counter from AR2. This circuit consists of three T-connected "D" flip-flops wired as a ÷8 ripple counter. In this configuration, the Q output of each stage is wired internally to its D input, with the Q output supplying the clock signal for the subsequent stage. In this way, the clock input to the first stage is divided by $2^3 = 8$, after propagating through the three-stage counter. A complete description of this circuit is in Section 4.2.

Since the high speed multiplexer requires an address generator which stabilizes more quickly than the ripple counter, a DFF NOR gate implemented synchronous counter, has been designed. The individual circuit is located on lot CD-33, and it is contained in both the multiplexer and demultiplexer circuits (CD-44 and CD-41). In the synchronous counter, all cells are gated on the same input clock pulse, so that the outputs of all stages stabilize virtually simultaneously after the propagation delay characteristic of only one of the cells.

Lot CD-44 is an 8-bit parallel input, 1-bit serial output multiplexer, with on-chip gating. Included on-chip in these circuits are a synchronous counter address generator and a latched output. Timing of the clock pulse to the output latch has been adjusted so that all propagation delays are accounted for before the multiplexer output is fixed, therefore preventing any false data from appearing at the output. Figure 5.1-14 is a schematic presentation of this circuit. While functionally identical to the multiplexer in AR2, this circuit has been completely redesigned to minimize voltage drop and hence power dissipation on the power supply bus lines. Slight modifications have also been incorporated to permit direct interfacing with the adjacent demultiplexer chip. Gate count of this circuit is 68.

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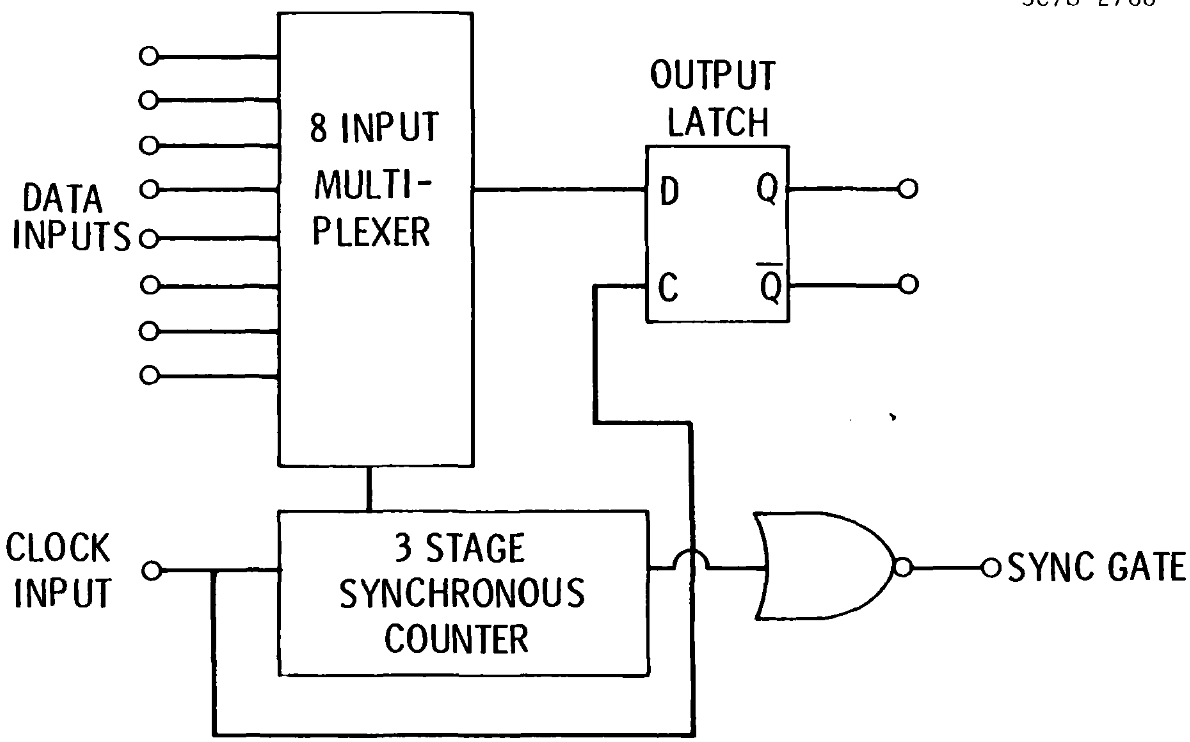
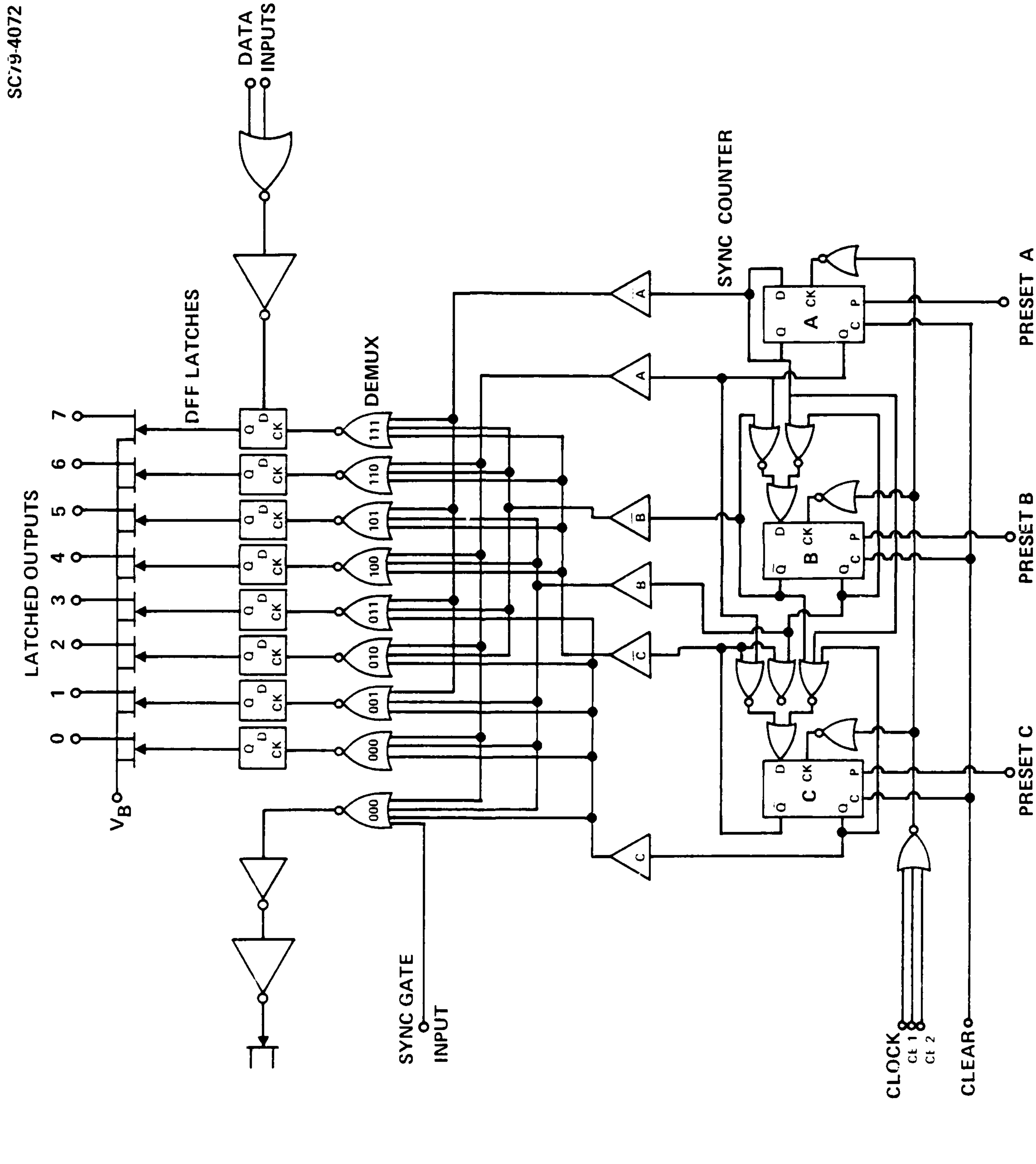


Fig. 5.1-14 Block diagram of the 8-input multiplexer (CD44).

Figure 5.1-15 represents a schematic diagram of the demultiplexer circuit in CD-41. This circuit is a 1-bit serial input, 8-bit parallel output demultiplexer, with source followers driving the contact pads. The synchronous counter was chosen to provide on-chip address generation and buffered to drive eight output latches as shown in Fig. 5.1-15. Gate count of the demultiplexer is 103.

The multiplexer (MUX) and demultiplexer (DEMUX) were implemented in adjacent lots of the CD chip and interconnected such that they can be tested individually or as a single unit. Figure 5.1-16 shows the photograph of the MUX and DEMUX pair on AR3. In order to achieve synchronization, proper gate delays were added to the clock signal, synchronous output and latched output of the MUX to drive the clock clear and data inputs of the DEMUX. A logic simulation computer program was used to analyze the interconnected MUX-DEMUX circuitry. The top portion of Fig. 5.1-17 shows the clock signal and the latched data output of the MUX as well as the synchronous clear input, 00 address signal and data input of the DEMUX. Note the time delay shown between the latched data output of MUX and data input of the DEMUX. The serial data were 01100101. The serial data input, address signals 00 and 01 as well as the latched output from address 00 and 01 of the DEMUX are given in the lower portion of Fig. 5.1-17, which shows the proper functioning of the MUX and latched DEMUX.

The overall design and content of the AR3 demonstration circuits presented above provide a significant step forward in GaAs planar IC technology. They will serve to further demonstrate the high density, low power and high speed capabilities of GaAs SDFL logic. It is expected that circuits will be fabricated from AR3 in the very near future. The evaluation of the performance of these circuits will require several months to complete. At that time, circuit design modification and circuit complexity needs will require the design of a fourth set of demonstration circuits.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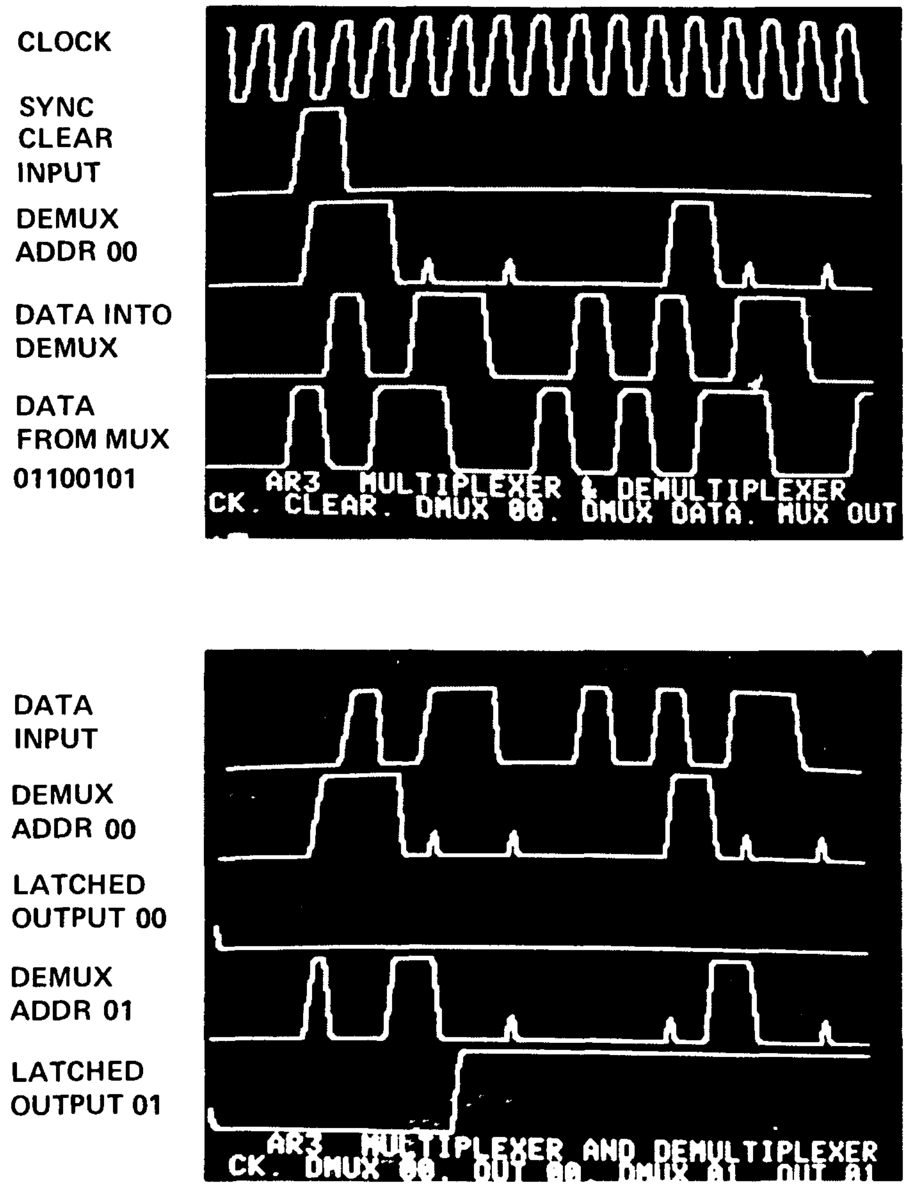
DATA INPUTS
SYNC COUNTER
DFF LATCHES
DEMUX
LATCHED OUTPUTS
7
6
5
4
3
2
1
0
V_B
SYNC GATE INPUT
PRESET A
PRESET B
PRESET C
CLOCK
Ct 1
Ct 2
CLEAR

SC79-4050



LOGIC SIMULATION OF MULTIPLEXER-DEMULTIPLEXER

Fig. 5.1-17 Logic simulation of multiplexer-demultiplexer.

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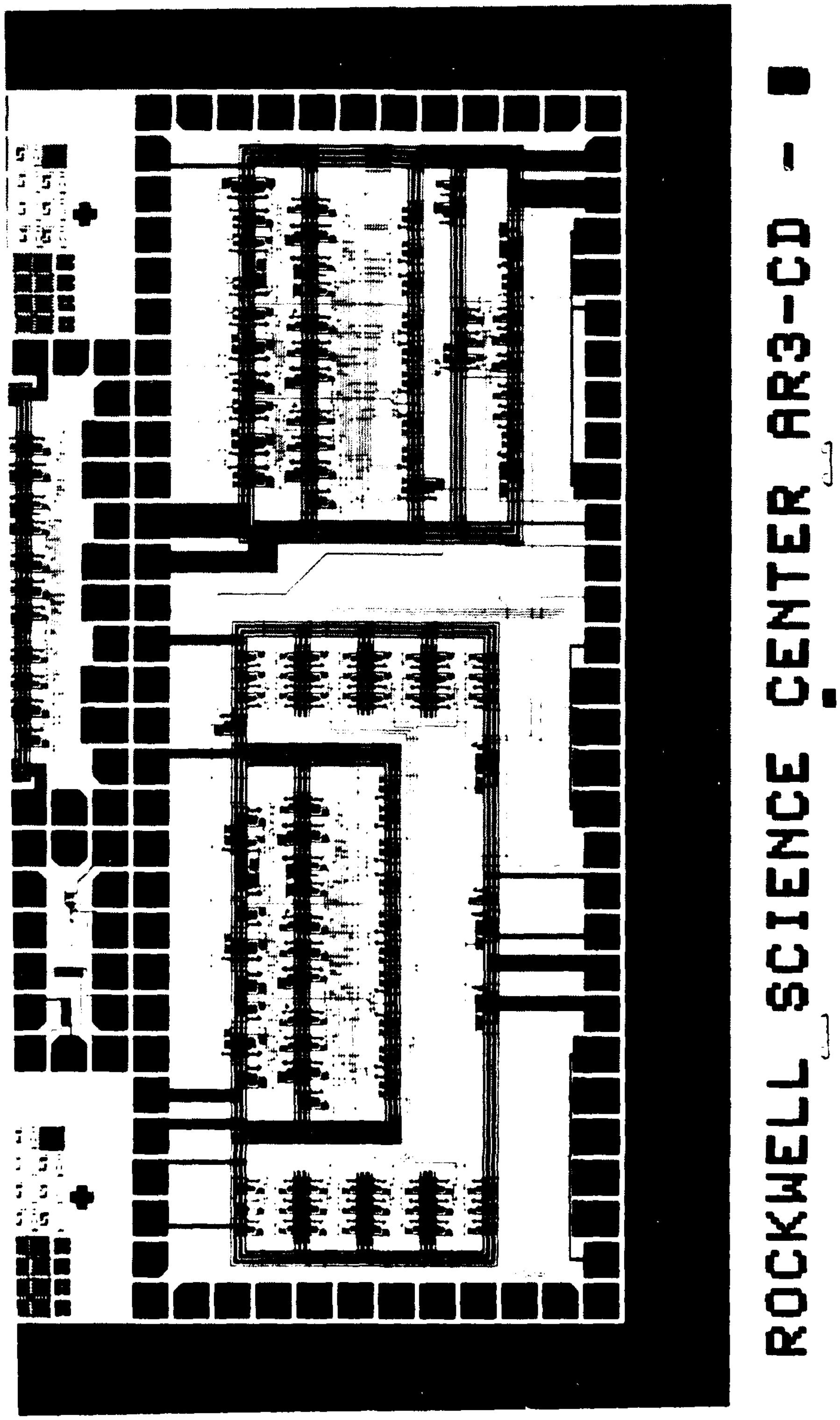

Fig. 5.1-16 Photograph of multiplexer-demultiplexer on CD41 and CD44 (from mask overlays).

5.2 GaAs FET Modeling (Cornell University)

The original GaAs FET modeling efforts, carried out in the first phase of this program, provided a relatively simple analytical model which agrees well with experimentally measured device parameters in the case of uniform doping profiles and high pinchoff voltages. Reasonable agreement with DC experimental data from the double-implanted, low pinch-off voltage FETS used in this program was also obtained at relatively large values of V_{GS}-V_P. However, the model does not accurately predict measured data at low levels.[1]

More recent modifications of the FET analytical model have permitted inclusion of nonuniform doping profiles typical of ion-implanted FET channels. Equations linking the transconductance (g_m) vs. gate voltage and the I_{DS} vs. gate voltage characterisics with the doping profile have been solved. Agreement with experimental data measured on typical ion-implanted logic FETs has been much better in the low I_{DS} range. Figure 5.2-1 shows a comparison of transconductance calculated from experimental data with that calculated from both the uniform and nonuniform doping profile models. Much better agreement can be seen near pinchoff for the nonuniform doping profile model than for the uniform doping profile model.

Further modifications to this nonuniform model will be implemented to include the effect of series resistance on the dc characteristics. Capacitance expressions will be recalculated to incorporate the nonuniform profile. Better agreement with experimental results in the V_{GS}-V_p < 0.5 V range is possible using the Shockley model; therefore a hybridization of the Shockley model and the above modified analytical model will be evaluated for circuit modeling purposes.

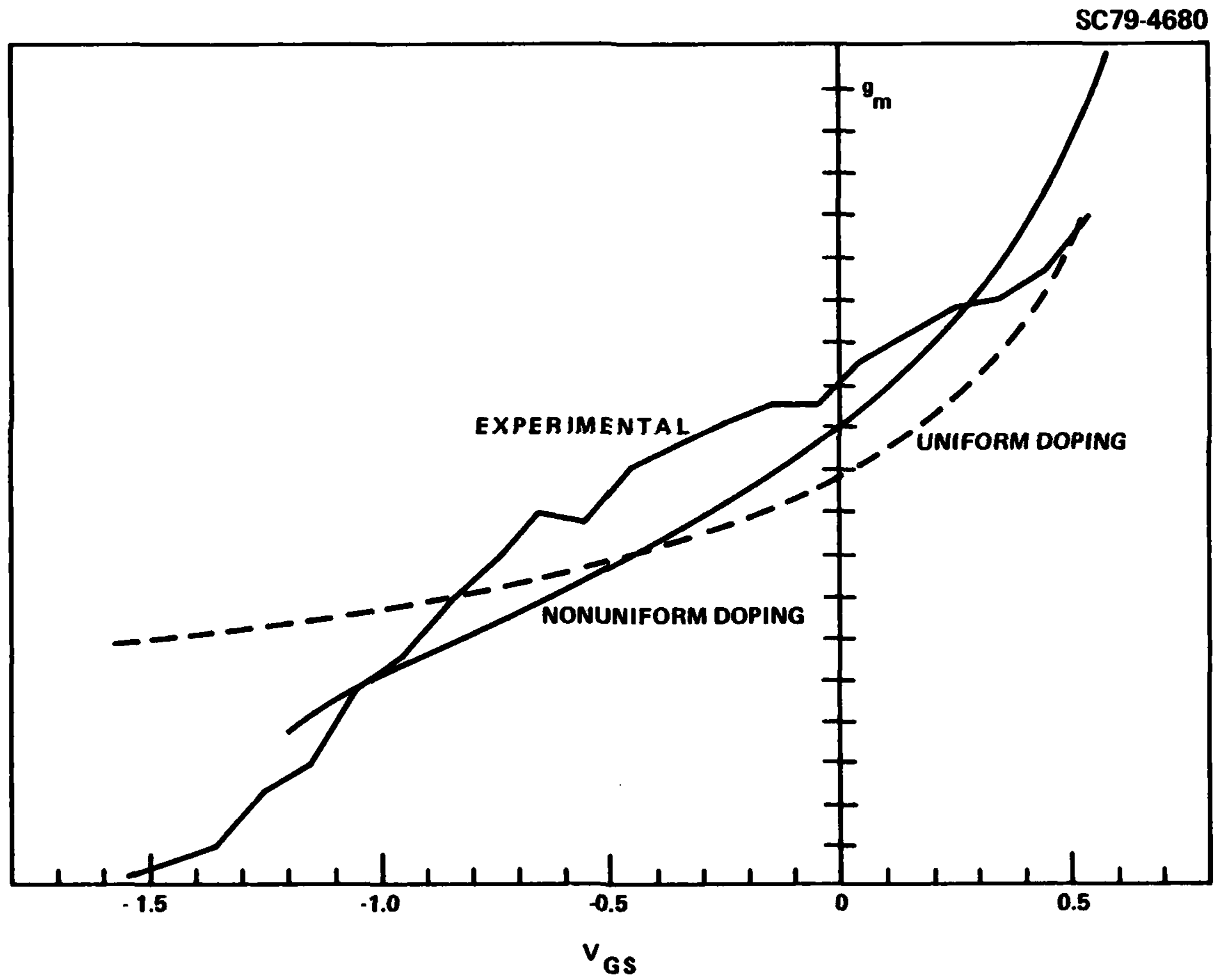

Fig. 5.2-1 Transconductance as a function of gate-source voltage for a 50μm FET. Calculated transconductances are shown for both the uniform and non-uniform doping profiles.

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